

Sayfe Kiaei

Work: WINTech & Connection One, GWC 302D; Mail Stop 8406; ASU, Tempe, AZ, 85287

Phone: 480-727-7761, email: sayfe@asu.edu

FIELDS OF SPECIALIZATION

RF IC design, Mixed-Signal IC Design, Wireless & Wireline Communication Systems

DEGREES

Ph.D., Electrical and Computer Engineering, Washington State University, 1987. Ph.D. Dissertation: "VLSI Implementation of Recursive Filtering and Estimation Blocks"

M.S., Electrical and Computer Engineering, Washington State University, 1984. Specialization in Computer Engineering and VLSI.

B.S.E.E., Electrical Engineering, Northeastern University/WSU, 1982.

IEEE Fellow, In the areas of Analog/Digital Mixed-Signal IC and RFIC design.

INDUSTRIAL POSITIONS

1993-2003 Motorola Inc., Senior Member of Technical Staff, Personal Communication Sector, Austin, Texas. Positions Held:

I. Platform Manager for RFIC Development, 1999-2001. Wireless Technology Center, PCS, Austin, Texas.

- **Bluetooth RFIC Development:** Responsible for the development of a single chip Bluetooth transceiver for the wireless handsets. In charge of the system architecture and design of front-end RF, down conversion IF stage, mixed-signal A/D-D/A, and baseband system development.
- **GPS-E911 Receiver RFIC:** Leading a team for the development of assisted GPS receiver for the wireless handset. Responsible for the system design, architecture, and evaluation board to test the A-GPS system in the handsets.
- **University relations:** Responsible for the development of collaborative research programs with several universities and the wireless integration technology center in Motorola. Responsible for funding research in the areas of Wireless Transceiver IC Design, RF, and mixed-signal and baseband system architecture.

II. System & Architecture Engineering, 1997-1999, Broadband Products Operations, Austin, TX 1997-99

- **Broadband Wireline System Architecture:** Formed and lead a new design team responsible for research and development of broadband communication transceivers. Primary responsibilities of the group was the development of next generation broadband

systems (ADSL, G.Lite), definition and specification of IC blocks, definition and design of transceiver blocks.

- **ADSL Transceiver:** Assisted in the development and completion of a single chip mixed-signal ADSL transceiver (*CopperGold[™]*). The transceiver contained Analog Front End (A/D, D/A, Hybrid), several custom accelerator blocks (DMT, modulation/demodulation, FFT, IFFT, echo cancelor, time domain equalizer, front-end constellation mapping, Trellis code modulation, Viterbi decoder) and an on-chip DSP core (Motorola 56k 24-bit DSP core).
- **xDSL Standards:** Represented Motorola in DSL Telecommunication standards including T1E1, International Telecommunication Unit (ITU), and the Universal ADSL Working Group (UAWG). Assisted in the definition and formation of G.Lite (ADSL Lite) standard in ITU and UAWG. Technical representative of Motorola to the ITU meetings in Geneva, Belgium, Sydney Australia, Hawaii, the United States, Canada, Italy, and France.

III. Baseband RF products DSP IC Engineer, 1993-1997, Land Mobile Products Sector, Plantation FL, and Austin Texas.

- Responsible for the development of custom baseband IC for wireless digital two-way radios. The baseband IC contained custom DSP blocks, A/D and D/A, and audio PA. The baseband IC is used in the next generation of digital two-way radios (new "*Talk about Radios*" announced Dec 99 at Las-Vegas consumer show), and in Japanese cellular systems (PHS).
- Developed fully-automated design process using C, MATLAB, Synopsis, and CADENCE tools to reduce the design cycle time from DSP block specification to FPGA test, timing verification, layout, and custom gate implementation.

1985-87 - Member of Research Staff, Boeing Co., Flight Systems Research and Technology Center, summer. Design Engineer, Hardware and CAD tool development for system control.

ACADEMIC POSITIONS

2001-Present - Professor and Director, Electrical Engineering Dept. Arizona State University, Tempe, AZ, 85287. Web site: www.connectionone.org

- Director of "Connection One: www.connectionone.org -- Center on Communication Circuits and Systems," Established new NSF/Industry center in Communication Circuits and Systems.

- Professor: Research and Teaching in Wireless transceiver design, RF transceivers, mixed-signal and Analog circuits. Projects funded by DARPA, JPL/NASA, Motorola Inc., Intel Inc., Texas Instruments, and other industry.

Adjunct Professor, Electrical and Computer Engineering Dept., The University of Texas, Austin, 1998-1999.

- Taught graduate courses: Introduction to Telecommunication System and Digital Communications. Member of two Ph.D. program committees in IC design and Telecomm.

Associate Professor (Tenured) 1987-1993, Electrical and Computer Engineering Department, Oregon State University

- Taught classes in VLSI system design, Electronics, DSP, Communications, and Wireless systems. Graduated 30 MS and Ph.D. students. Research in VLSI & DSP, mixed-signal IC design, communication.

Co-Director, Center for the Design of Analog/Digital IC's (CDADIC), 1988- 1997.

- *CDADIC* is a National Science Foundation University-Industry research center (UIRC) focused on mixed-signal IC research. Assisted in the establishment of the center in 1987 with Washington State University. Attracted several new industrial members and NSF to the center. Responsible for managing the research funds, assisted in the evaluation of new research projects, and was a liaison between the industrial members and the universities for technology transfer.
- *CDADIC* members include four universities (*Oregon State University, University of Washington, Washington State University, University of N.Y. Stony Brook*), over 25 Electronics companies, and the National Science Foundation. The annual research budget is over one million dollars.

Post Doctoral Lecturer, Electrical and Computer Engineering, Washington State University, 1986.

Research & Teaching Assistant, Washington State University 1982-1987.

CONSULTING

Boeing Commercial Aircraft (85/86), Tektronix Inc. (87/88), Motorola Inc. (95/96), HP (90-93), Intel (02/03), Sensor Technologies & Systems (1/04-Present), Expert Witness on RF IC Design and Mixed-Signal IC Design.

AWARDS

- **IEEE Fellow, For contributions in Mix-Signal Design**
- **Global Standards Award**, For contributions in the International Telecommunication Unit (ITU) for Asymmetric Digital Subscriber Line (ADSL) G.Lite Standards. Motorola Inc., 1999.

- **10X Cycle Reduction Award**, for development of new IC design process from DSP algorithm to IC layout, Motorola Inc., 1995.
- **IEEE Darlington Award, IEEE Circuits and Systems Society Best Paper Award**, 1995. For “Characterization and Comparison of CMOS FSCL Circuits with Conventional CMOS for mixed-signal ICs,” Published at: *IEEE Trans. on Circuits and Systems II, Sept. 93*.
- **Carter Best Teaching Award**, College of Engineering Best Teacher Award, Oregon State University, 1992. For “*outstanding and inspirational teaching in the College of Engineering*”. Award is selected by the confidential vote of all of the undergraduate students in the College of Engineering among over 125 professors in the College.
- **Industrial University Fellowship (IUF) Award**, National Science Foundation, 1993.
- **Research Initiation Award**, National Science Foundation, 1990-93.
- **Outstanding Graduate Student Scholarship**, Azur-Data Inc. WSU, 1984.

FUNDED RESEARCH PROJECTS

- New Techniques for Time Measurement Circuits; BAE Systems; Organized Research; February 2006; \$36,400
- SRC Fellowship; Semiconductor Research Corp; October 2005; \$2,050
- Connection One - Communications Circuits and Systems Research Center; NSF-Engineering; August 2005; \$30,000
- Radhard by Design - MRC/DARPA; Mission Research Corporation; July 2005; \$940,095
- Connection One- Annual Membership; Texas Instruments; Freescale Semiconductor, General Dynamics C4 Systems, SpaceMicro, Ridgetop Group, SiRF Technology; \$285,000; July 2005
- SRC Fellowship; Semiconductor Research Corp; October 2004; \$16,600
- Connection One- Communications Circuits and Systems Research Center; NSF-Engineering; August 2004; \$176,000
- Connection One Compendium Supplement; NSF-Engineering; August 2004; \$10,772
- Connection One – Annual Membership; Texas Instruments, SiRF, Intel, Ridgetop Group; July 2004; \$185,000
- Nano-Mechanical RF Band pass resonator for 2GHz RF Applications, Defense Advance Project Agency (DARPA), \$2 Million, 2002-2005
- Design of Multi-Standard RF Front-End Circuits, Intel Corporations, \$300K, 2002-2005
- Connection One: Center for Communication Circuits and Systems, National Science Foundations, \$400K; 2002-2007.
- On-Chip Power Management IC’s for Wireless System on a Chip, NSF Connection One Center, \$54K, 2002-2003

- Multi-Standard LNA Design, NSF Connection One Center, \$54K, 2002-2003
- Mix-Signal and RFIC Design for SOC, Motorola Inc, \$320K, 2001-2002
- DC-DC regulators and RF IC on-chip Power management, Texas Instruments; \$100K
- ASU Mix-Signal Center, Texas Instrument, \$150K, 2000-2002
- Connection One industrial contributions, \$300K, 2002-2003
- Undergraduate Analog Electronics Lab Equipment, Tektronix, \$750K, 2002
- Graduate RA Fellowships, Texas Instruments, \$45K, 2002
- Multi-Input Multi-Output Transceiver Design, AZ State 301, \$225K, 2002-2003
- Connection One Center, AZ State 301, \$150K, 2002-2003
- Ultra-Wideband Transceivers, SRC (Semi-conductors research Corp), \$225K, 2001-2003
- Adaptive Compensation of Analog circuits imperfections using DSP methods, *National Science Foundation* \$60K, 1996 (tie project with UC San Diego NSF center) (Co-PI Gabor Temes)
- Adaptive Compensation of Analog circuits using DSP methods, *Center for the Design of Analog/Digital IC's (CDADIC)*, \$60K, 97-98 (Co-PI Gabor Temes)
- Low Power IF processing for Direct Digital Transceivers, *Motorola Inc*, \$100K, 93-96.
- Direct Conversion and Sub-sampling circuits for Wireless Transceivers, *CDADIC*, \$120K, 96.
- Testable Analog Circuits, *NSF, Mixed-Signal IC design Center at University of California, San Diego, and CDADIC*, 1991-93, \$75K. (Co-PI Gabor Temes).
- Hewlett-Packard Faculty Chair position in Mixed-Signal IC, HP, 1995-97, \$500K (Co-PI D. Allstot)
- Faculty Industry Fellowship, *National Science Foundation, Motorola Inc*, \$120K, 93-94.
- Synthesis and Automatic Derivation of Multi-Rate VLSI Arrays for DSP Algorithms, *National Science Foundation, Research Initiation Award (RIA)*, 90-93.
- Research Experience for Undergraduate Students, *National Science Foundation, Research Initiation Award (RIA)*, \$10K, 1990-93.
- CDADIC Center Co-Director, *National Science Foundation*, \$450K (\$50K/ year), 1988-97.
- Low-Noise Source Coupled Logic (SCL) for Mixed-Mode IC's, *CDADIC*, \$200K, 1988-1992.
- Decimation Filters for A/D Noise Enhancements, Tektronix, Inc., \$10K, 1988.
- Various grants for IC Fabrication (DARPA/MOSIS, VLSI), testing equipment (Tek, HP), DSP system development (TI, Motorola), ranging in various amounts up to \$100K/year. 1988-1997.

PROFESSIONAL RECOGNITION

- IEEE Fellow, 2002-Present
- IEEE Senior Member, 1993-Present, IEEE Member 1987-1992.
- IEEE Faculty Advisor, Oregon State University, 1987-1990

IEEE Editorials

- Associate Editor, IEEE Transactions on VLSI, Jan 2001-Present.
- Editor, Feature Issues on “Circuits for Wireless and Wireline Communications,” IEEE Comm. Magazine, April 1999.
- Editor, Special Issue on: "Radio Frequency IC Design," IEEE Transactions on Microwave Theory and Techniques, Dec. 1998.
- Editor, Special Issue on: “Low-Power Wireless Communication Systems,” IEEE Transactions on Circuits and Systems-II, June 1997.
- Associate Editor, IEEE Transactions on Circuits and Systems-II, 1993-1996.

Conference Organizations

- Technical Program Member, IEEE ISCAS 2003
- Executive Board Member, RFIC 2003
- Technical Program Chair, IEEE International Sym. on Circuits and Systems, Phoenix, AZ, 2002.
- General Chair, Radio Frequency IC (RFIC) Symposium, Seattle, WA, 2002.
- Technical Program Chair, RFIC Symposium, Phoenix, AZ, 2001.
- Finance Chair, RFIC symposium, Boston, Ma, 2000.
- Publicity Chair, RFIC symposium, Los Angeles, CA, 1999.
- Transactions Chair, RFIC symposium, Baltimore, MD, 1998.
- General Chair, Int. Sym. on Low-Power Electronics and Design (ISLPED), Monterey, CA, 97.
- Technical Program Chair, Int. Sym. on Low-Power Electronics and Design, Monterey, CA, 96.
- Executive Committee Member, Int. Symp. On Low-Power Electronics and Design, 96-2000.
- Steering Committee Member, RFIC symposium, 1996-Present.
- Technical Program Committee Member, GLS VLSI 1998, Lafayette, Louisiana, 1998
- Technical Program Committee Member, VLSI Design 98, Chennai, India, Jan. 1998.
- Technical Program Committee Member, ICECS, Lisbon, Portugal, 98.
- Technical Program Committee Member, IEEE Int. Symp. On Circuits and Systems, 1995-97.
- Technical Program Committee Member, Application Specific Array Processing, 1995-97, 2000

- Technical Program Committee Member, Vehicular Technology Conference, 1995-97.
- Technical Program Committee Member, Inter. Conf. on Intelligent Information Systems, D.C., 1994-95.
- Technical Program Committee Member, IEEE Pacific Rim Conference on Communications & Computers, Victoria, BC, Canada, 1991.

Invited talks, Panelist, Session Chairs, Workshop Speaker

- Workshop speaker: "Communication and Signal Processing Circuits for ADSL/VDSL Systems," International workshop on design of mixed-mode integrated circuits and applications, Guanajuato, Mexico, 1998.
- Workshop speaker: "Fundamentals of Broadband ADSL Systems," SuperComm 98, Atlanta, Ga.
- Organizer and Workshop speaker, "RF IC design," Five day industrial short course on RF IC design, Portland, OR, 1995-1998.
- Organizer, "Wireless Transceiver & RF design," Five day industrial short course, Mead Electronics, Swiss Federal Institute of Technology, Lausanne, Switzerland, (also held at Monterey, CA), 1994-1995.
- Panel chair and organizer, "Low Power Breakthroughs: CAD Tools or Electronics?" International Symposium on Low-Power Electronics and Design, Monterey, CA, Aug 1996.
 - Panelists: James Burr (Sun Micro), Laszlo Gal (Motorola), Ramsey Haddad (Synposys Inc.), Jan Rabaey (UC Berkeley), Bruce Wooley (Stanford University)
- Panel member, "Low Power Wireless & RF Design," Int. Sym. on Low-Power Electronics and Design, Aug 95.
 - Panelists: Sayfe Kiaei (Motorola), Dan Dobberpuhl (DEC), Paul Solomon (IBM Corp.), and Paul Gray (UC Berkeley).
- Full day Tutorial: "Low-Power RF Design," Design Automation Conference (DAC), Anaheim, CA, June 1997.
- Special session organizer, "Wireless Communication Systems," IEEE Int. Symp. On Circuits, and Sys., Seattle, WA, 1995.
- Special Session Organizer, "VLSI and Signal Processing," IEEE Pacific Conference on Communications, Computers, and Signal Processing, Victoria, BC Canada, 1991.
- Session Chair in various conferences (ISCAS, ICASSP, Low-Power Symposium, RF IC Conference, ICC, Application Specific IC's, IMS), 1987-Present.

PATENTS, PUBLICATIONS

Patents & Disclosures

1. S. Kiaei, N. Darbanian, Shahin Farahani, .S. Provisional Application No. 60/428,432, # 51579P/DMC/A59, “ CVB RF Models,
2. S. Abedinpour and S. Kiaei, “Monolithic Supply-Modulated RF Power Amplifier and DC-DC Power Converter IC,” M3-047.
3. S. Abedinpour and S. Kiaei, “Integrated ZVS Synchronous buck DC-DC Converter with Adaptive Control for Improved ZVS Performance,” ASU Formal Application , M2-086.
4. S. Taleie, B. Bakkaloglu and S. Kiaei, “Finite Impulse Response Digital-to-Analog Converter”, Provisional Patent Application, AZTE Case Nr: M6-020.
5. “Low-Noise MOS Folded Source Coupled Logic (FSCL) for Mixed-Signal ICs” US Patent # 5,149,992. This technology is a key component in various low-noise mixed-signal IC's being developed by a number of semi-conductor corporations such as with volumes well over 10-15 millions units per year. Application ranges from RF/IF Frequency Synthesizers, receiver correlation, Ultra-Wide Band receivers, A/D Decimation filters, etc.
6. “Circuits and Systems for Powers of Two Wave Digital Filters,” Motorola Inc., 1995
7. “Direct Digital Demodulation for Narrow band signals,” Motorola Inc., 1996
8. “Capacity Maximized TEQ block for ADSL”, Motorola Inc., 97.
9. “Fast LMS Equalization with adaptive step size for TEQ,” Motorola Inc., 98.
10. “Peak-to-Average (PAR) reduction for DMT system,” Motorola Inc., 98.
11. Three new disclosures on GPS and Bluetooth (Motorola Confidential until it’s public).

Telecommunication Standards Contributions

1. “Spectral Compatibility of ADSL: Frequency Overlap vs. FDM,” T1E1, Dec. 97.
2. “Echo Cancellation for G.Lite Universal ADSL,” Universal ADSL Working Group, Atlanta, GA, Jan 98.
3. “8-bit QAM Constellation effects on reach for universal ADSL,” Universal ADAL Working Group, Atlanta, GA, Jan 98.
4. “Trellis Code Modulation coding gain,” Universal ADAL Working Group, Atlanta, GA, Jan 98.
5. “Monte Carlo Modeling and simulation of twisted pair wiring,” Universal ADAL Working Group, Atlanta, GA, Jan 98.

6. "Overlap Upstream/Downstream spectral allocation for ADSL," International Telecommunication Unit, Chicago, March 98.
7. "Echo Cancellation for ADSL," International Telecommunication Unit, Antwerp, Belgium, 98.
8. "Performance of Echo Cancellation ADSL system in the presence of Near End Cross Talk (NEXT)," International Telecommunication Unit, Honolulu, Hawaii, June 98.
9. Presentations and editorials at various ADSL standards: ITU, UAWG, and T1E1, 97-99.

Journal Papers Submitted (in the review process)

1. "Phase & Gain (I/Q) Correction in Homodyne Receivers", Submitted to the IEEE Trans. on Comm. [S. Kiaei, J. Vogel, M. Scarpa].
2. "BER of Differentially Detected $\pi/4$ DQPSK Distorted by I/Q Phase Imbalance", Submitted to the IEEE Transactions on Selected Topics in Communications. [S. Kiaei, J. Vogel, M. Scarpa, J. Stonick]

Journal Papers published (or accepted)

3. "Channel Shortening For Discrete Multi-tone Transceivers To Maximize Channel Capacity," IEEE Transactions for Signal Processing, Accepted, under revision, publication date TBD for 2001 [G. Arslan, B. Evans, S. Kiaei]
4. "Capacity Optimization for ADSL System," IEEE Transactions on Communications, Accepted, Publication date TBD for 2001. [N. Lashkarian, S. Kiaei]
5. "Frequency Off-Set Circuits for OFDM Systems", IEEE Transaction on Communications, Dec 2000. [N. Lashkarian, S. Kiaei].
6. "Noise Considerations for Mixed-Signal RF IC Transceivers," ACM Transaction on Wireless Networks, Vol. 4, pp. 41-53, 1998. [S. Kiaei, D. Allstot, N. Verghese, K. Hansen].
7. "A triangularly weighted zero-crossing detector providing delta-sigma frequency-to-digital conversion", *IEE Electronics Letters*, vol.33, no.13, pp.1121-1122, June 1997. [M. Hovin, S. Kiaei, T.S. Laude]
8. "Adaptive Multi-user Detector For Asynchronous DS- CDMA In Raleigh Fading," IEEE Transactions on CAS-II, pp. 468-473, June 97. [A.K. Dutta, S. Kiaei]
9. "Multi-Rate Transformation of Recurrence Equations for Regular VLSI Arrays, " Application Specific Array Processors, IEEE Press, 1994. [L. Aihua, S. Kiaei]
10. "Analog Logic Techniques," IEEE Circuits and Devices Magazine, pp. 12-21, May 1993. [S. Kiaei, D. Allstot, R. Zele]
11. "Overlapping Transformation for Time-Area Optimal VLSI arrays for Toeplitz Matrices," J. of Computer and Software Engineering, Vol. 3, #4, pp. 461-481, June 95. [S. Kiaei, Yuepeng Zheng]
12. "Characterization and Comparison of CMOS FSCL Circuits with Conventional CMOS Logic for Hybrid ICs," IEEE Trans. on Circuits and Systems, Sept. 93. [S.H. Chee, S. Kiaei, D. Allstot]

13. "Low Noise Logic for Mixed-Mode VLSI Circuits, Journal of microelectronics, " Vol. 23, No. 2, pp. 103-115, April 1992. [S. Kiaei, D. Allstot]
14. "Enhancement Source-Couple Logic ESCL," IEEE Trans. on Circuits, and Systems II: Analog and Digital Signal Processing, Vol. 39, No. 6, pp. 399-402, July92. [M. Maleki, S. Kiaei]
15. "Synthesis of Complex FSCL Blocks for Mixed Mode Systems," IEEE J. Solid State Circuits, Vol. 27, No. 8, pp. 1157-1168, Aug 1992. [S. Maskai, S. Kiaei, D. Allstot]
16. "Adaptive self-correcting D-S Modulators," IEE Electronics Letters, Vol. 28, No. 14, pp. 1288-1290, July 92. [S. Abdenadher, S. Kiaei, G. Temes, R. Schreier]
17. "On-line Adaptive Digital Correction of Dual-Quantization Delta-Sigma Modulators," IEE Electronics Letters, Vol. 28, No. 16, pp. 1511-1513, July 92.[Y. Yang, R. Schreier, G. Temes, S. Kiaei]
18. "Piecewise Linear Schedules for Recurrence Equations," VLSI Sig. Proc. VI, IEEE Press, 1992. [S. Rajopadhye, L. Mui, S. Kiaei]
19. "Automatic Synthesis and Derivations of VLSI Architectures for Recursive IIR Digital Filters," CAD for VLSI Design, 1990. [S. Kiaei, S. Rajopadhye]
20. "VLSI Design of Wavefront Array Processors for Recursive Filters," VLSI Signal Processing II, IEEE Press, pp. 152-164, 1988. [S. Kiaei, U.B. Desai]

Journal Editorial Articles

21. "RFIC Design," IEEE Transactions on Microwave Theory and Techniques, v. 46, pp. 2180-2183, Dec. 98. [S. Kiaei, R. Gupta]
22. "Circuits for Wireless and Wireline Communications," IEEE Comm. Magazine, April 1999. [S. Kiaei]

Conference Publications

1. S. Kiaei, S. M. Taleie, B. Bakkaloglu, "Low-power high-Q NEMS receiver architecture", *IEEE International Symposium on Circuits and Systems*, Vol.5, 23-26 May 2005 Page(s):4401 - 4404
2. Kiaei, Overview of Transmit and Linear PA Up-converters, Vol 5, May 05; RFIC 2005, Workshops, PP. 28-45.
3. S. Kiaei, RF Design of Up and Down converters, S. Kiaei, Vol. 5, May 05, RF Building Blocks workshop, PP. 45-68. Location: Long Beach Convention Center, Room 102AB
4. S. Kiaei, IMS 2005, DC/DC converters and Noise Shaping Techniques for Switched-Mode DC/DC Converters for RF Transceivers, Vol. 5, May 05, Monolithic Power Management workshop, PP. 98-112.
5. "Simulation Of Nonlinear Systems With Sparse Input Vectors Using CRC Techniques" [S. Farahani, N. Darbanian, S. Kiaei]
6. "Linear RF Polar Modulated SiGe Class E and F Power Amplifiers," [Kitchen, J.; Deligoz, I.; Kiaei, S.; Bakkaloglu, B.] 2005.

7. "Polar Modulated Power Amplifier," [Deligoz, I.; Kitchen, J.; Kiaei, S.] 2005.
8. "A Bandpass Delta Sigma RF-DAC with Embedded FIR Reconstruction Filter," International Solid State Circuits Conference (ISSCC) 2006 [Taleie, S.M.; Copani, T.; Bakkaloglu, B.; Kiaei, S.]
9. "An Educational Tool and Teaching Guidelines for Nonlinear Systems with Sparse Inputs" [S. Farahani, N. Darbanian, S. Kiaei]
10. "Automated Synthesis Tools for Analog & RF IC Software Definable Tranceivers" [S. Farahani, N. Darbanian, S. Kiaei]
11. "Compressed Vector-Based Spectral Analysis Technique for RF Nonlinear Analysis and Simulation of Circuits and Systems," Proc. of IEEE WAMI Conference, Clearwater, FL, June 2004. [S. Farahani, N. Darbanian, S. Kiaei]
12. "A SiGe BiCMOS 0.18 μ m Multi-Mode RF front-end for GSM 1.8, GPS, and WCDMA Applications," Proc. of IEEE WAMI Conference, Clearwater, FL, June 2004. [N. Darbanian S. Farahani, A. Afsahi, H. Song, S. Kiaei, M. Smith]
13. "Delta-Sigma Data Converters for Wireless Applications," Proc. of 2003 International Workshop on ADC's, June 2003. [Chaudhuri, Bikram, Kiaei, S.]
14. "A Pseudo-Concurrent 0.18 μ m Multi-Band CMOS LNA," Proc. of 2003 IEEE MTT-S International, June 2003. [Lavasani, S.H.M.; Chaudhuri, B.; Kiaei, S.]
15. "Monolithic Supply Modulated RF Power Amplifier and DC-DC Power Converter IC," Proc. of 2003 IEEE MTT-S International, June 2003. [Abedinpour, S.; Deligoz, K.; Desai, J.; Figiel, M.; Kiaei, S.]
16. "A Novel Low Phase Noise 1.8V 900MHz CMOS Voltage Controlled Ring Oscillator," Proc. of ISCAS '03 Volume: 3, May, 2003. [Badillo, D.A.; Kiaei, S.]
17. "Monolithic Distributed Power Supply for a Mixed-Signal Integrated Circuit," Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium on, Volume: 3, 2003 [Abedinpour, S.; Kiaei, S.]
18. "A Pseudo-Concurrent 0.18 μ m Multi-Band CMOS LNA," Radio Frequency Integrated Circuits (RFIC) Symposium, 2003 IEEE, June 2003 [Lavasani, S.H.M.; Chaudhuri, B.; Kiaei, S.]
19. "Parasitic-aware synthesis of RF CMOS switching power amplifiers," Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on, Volume: 1, 2002 [Kiyong Choi; Allstot, D.J.; S. Kiaei]
20. "Monocycle shapes for ultra wideband system," Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on, Volume: 1, 2002, PP. 597 –600, [Xiaomin Chen; Kiaei, S.]
21. "An all-digital programmable digitally-controlled-oscillator (DCO) for digital wireless applications," Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on, Volume: 4, 2002, [Abdollahi, S.R.; Kiaei, S.; Bakkaloglu, B.; Fakhraie, S.M.; Anvari, R.; Abdollahi, S.E.]
22. "Optimum equalization of multicarrier systems: a unified geometric approach Communications, IEEE Transactions on, Volume: 49 Issue: 10, Oct. 2001; Page(s): 1762 –1769, [Lashkarian, N.; Kiaei, S.]

23. "Equalization for Discrete Multitone Transceivers to Maximize Bit Rate," IEEE Transactions on Signal Processing, Volume: 48, Issue:12, Dec. 2001; Pgs. 3123-3135, [Arslan, Evans, Kiaei]
24. "Performance of Differentially Detected DQPSK in the presence of I/Q Phase Imbalance," International Symposium on Circuits and Systems, Zurich, Switzerland, June 2000. [M. Scarpa, J. Vogel, J. Stonick, S. Kiaei]
25. "Globally Optimal ML Estimation of Timing and frequency offset in OFDM Systems," International Communications Conference, New Orleans, Louisiana, 2000. [N. Lashkarian, S. Kiaei]
26. "Minimum variance unbiased estimation of frequency offset in OFDM systems, a blind synchronization approach." Int. Conf. On Acoustics, Speech and Signal Processing, Istanbul, Turkey, 2000. [N. Lashkarian, S. Kiaei]
27. "Optimum Channel Shortening for Multicarrier Transceivers, " Int. Conf. On Acoustics, Speech and Signal Processing, Istanbul, Turkey, 2000.[G. Arslan, B. Evans, S. Kiaei]
28. "Class of Cyclic-Based Estimators for Frequency-Offset Estimation of OFDM Systems," IEEE Transactions on Communications, Volume: 48, Issue:12, Dec. 2000; Pgs. 2139-2149, [Lashkarian, Kiaei]
29. "Optimum Equalization of Multi-Carrier Systems Via Projection onto Convex Set," International Communication Conference, Vancouver, British Columbia, Canada, 1999. [N. Lashkarian, S. Kiaei]
30. "BER of Differentially Detected $\pi/4$ DQPSK in the Presence of Quadrature Gain Imbalance" IEEE Wireless Communications and Networking Conference, Sept. 1999. [M. Scarpa, J. Vogel, J. Stonick, S. Kiaei]*
31. "Fast Equalizers for Finite Length MMSE Equalization with Application to DMT ADSL System," Int. Conf. On Acoustics, Speech and Signal Processing, vol. 5, pp. 2753-2756, Phoenix, AZ, 1999. [N. Lashkarian, S. Kiaei]
32. "Communication and Signal processing Circuits for ADSL/VDSL system," international workshop on design of mixed-mode integrated circuits and applications, Guanajuato, Mexico, July 1998. [S. Kiaei]
33. "Analysis of Adaptive CMOS Down Conversion Mixers," Proceedings of the 8th Great Lakes Symposium on VLSI, Feb. 1998. [Sandalci, C.K.; Kiaei, S.]
34. "DC offset correction for direct conversion transceivers," Great Lake VLSI Symposium, Lafayette, Louisiana, 1998. [C. Sandalci, S. Kiaei]*
35. "Fundamentals of ADSL system," SuperComm, Atlanta, GA, June 1998. [S. Kiaei]
36. "Low-Power RF Design," Design Automation Conference (DAC), Anaheim, CA, June 1997. [S. Kiaei]
37. "Adaptive Multi-user Detector for Asynchronous DS-CDMA in Rayleigh Fading," Transactions on Circuits and Systems II: Analog and Digital Signal Processing, June 1997. [Dutta, A.K.; Kiaei, S.]
38. " Δ - Σ Frequency-to-Time Conversion by Triangularly Weighted ZC Counter," International Symposium on Low Power Electronics and Design, Aug. 1997. [Hovin, M.; Kiaei, S.; Lande, T.S.]

39. "Introduction to the Special Issue on Low Power Wireless Communications," IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, June, 1997. [Kiaei, S.; Friedman, E.G.]
40. "Low Power Frequency-to-Time Conversion for Cellular Systems Using Predictive Zero-Crossing," 1997 IEEE 47th Vehicular Technology Conference, May 1997. [Dutta, A.K.; Kiaei, S.; Talwalkar, S.A.]
41. "Triangularly Weighted Zero-Crossing Detector Providing $\Sigma\Delta$ Frequency-to-Digital Conversion," Electronics Letters, Volume: 33, Issue: 13, June 1997. [Hovin, M.E.; Lande, T.S.; Wisland, D.T.; Kiaei, S.]
42. Pages:1121 - 1122
43. "Low-Power Delta-Sigma Time-to-Digital Conversion," *Proc. 1997 International Symposium on Low Power Electronics and Design*, pp. 52-56, Monterey, CA, 1997. [M. Hovin, S. Kiaei, T.S. Laude]
44. "Modified Adaptive Multi-user Detector for DS-CDMA with Fading," 47th Vehicular Technology Conference, VTC 97, Phoenix, AZ, May 97. [A. Dutta, S. Kiaei]
45. "Predictive Zero-Crossing Frequency Discrimination for Cellular Systems, Part I and II." 47th Vehicular Technology Conference, VTC 97, Phoenix, AZ, May 97. [A. Dutta, S. Kiaei]
46. "CDMA Multi-user Cancellation," ", Int. Conf. On Acoustics, Speech and Signal Processing, Munich, Germany, April 97. [A. Dutta, S. Kiaei]
47. "Digitally Correcting Schemes for Oversampled A/D," Int. Symp. On Circuits and systems, London, UK, 1994. [S. Abdenadher, S. Kiaei, G. Temes, R. Schreier]*
48. "Multi-Rate Transformation of Recurrence Equations," Int. Conf. on ASAP, Venice, Italy, Oct. 1993. [Li Aihua, Y. Zheng, S. Kiaei]
49. "Adaptive Digital Correction for Dual Quantization /spl Sigma/-/spl Delta/ Modulators," IEEE International Symposium on Circuits and Systems, May 1993. [Kiaei, S.; Abdennadher, S.; Temes, G.C.; Yang, Y.]
50. "Analog Logic Techniques Steer Around the Noise," IEEE Circuits and Devices Magazine, Volume: 9, Issue: 5, Sept. 1993; Pages:18 – 21 [Allstot, D.J.; Kiaei, S.; Zele, R.H.]
51. "Folded Source-Coupled Logic vs. CMOS Static Logic for Low-Noise Mixed-Signal ICs," IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, Sept. 1993. [Allstot, D.J.; San-Hwa Chee; Kiaei, S.; Shrivastawa, M.]
52. "Multi-Rate Transformation of Directional Affine Recurrence Equations," International Conference on Application-Specific Array Processors, Oct. 1993. [Zheng, Y.; Kiaei, S.]
53. "Adaptive self-correcting $\Sigma-\Delta$ modulators," International Conference on microelectronics, Tunisia, 1992. [S. Abdenadher, S. Kiaei, G. Temes]*
54. "Adaptive Self-Calibrating Delta-Sigma Modulators," Electronics Letters, Volume: 28, Issue: 14, 2 July 1992; Pages: 1288 – 1289. [Abdennadher, S.; Kiaei, S.; Temes, G.; Schreier, R.]
55. "Enhancement Source-Coupled Logic for Mixed-Mode VLSI Circuits," IEEE Transactions on

Circuits and Systems II: Analog and Digital Signal Processing, Volume: 39, Issue: 6, June 1992; Pages: 399 – 402. [Maleki, M.; Kiaei, S.]

56. "On-line Adaptive Digital Correction of Dual-Quantization Delta-Sigma Modulators," Electronics Letters, Volume: 28, Issue: 16, 30 July 1992; Pages: 1511 – 1513 [Yaohua Yang; Schreier, R.; Temes, G.C.; Kiaei, S.]
57. "Piecewise Linear Schedules For Recurrence Equations," Workshop on VLSI Signal Processing, Oct. 1992. [Rajopadhye, S.; Mui, L.; Kiaei, S.]
58. "Synthesis Techniques for CMOS Folded Source-Coupled Logic Circuits," IEEE Journal of Solid-State Circuits, Aug. 1992. [Maskai, S.R.; Kiaei, S.; Allstot, D.J.]
59. "A Folding Transformation for VLSI IIR Filter Array Design," Proc. of International Conference on Acoustics, Speech, and Signal Processing, Toronto, Canada, pp. 1237-1240, May 1991. [S. Rajopadhye, S. Kiaei]
60. "Systematic Derivation of Multi-Rate VLSI Arrays for the Solution of Toeplitz Matrices," IEEE Great Lakes Symposium on VLSI, March 1991. Proc. of IEEE Pacific Rim Conference on Communications, Computers, and Signal Processing, Victoria, BC, Canada, pp. 623-626, May 1991. [S. Kiaei]
61. "CMOS Source-Couple Logic for Mixed-Mode VLSI," Proc. of International Symposium on Circuits and Systems, New Orleans, Louisiana, pp. 1608-1611, May 1990. [S. Kiaei, S.H. Chee, D. Allstot]
62. "VLSI Design of Multi-Rate Arrays," Proc. of International Conference on Acoustics, Speech, and Signal Processing, New Mexico, pp. 1049-1052, 1990. [L. Aihua, S. Kiaei]
63. "Comparison of Low-Noise Current-Mode Logic Circuits for High Performance Mixed-Mode Applications," Proc. of International Symposium on Circuits and Systems, New Orleans, Louisiana, May 1990. [S. H. Chee, S. Chow, S.S. Lee, S. Kiaei, D. Allstot]
64. "VLSI Design of Dynamically Reconfigurable Array Processors-DRAP," Proc. of International Conference on Acoustics, Speech, and Signal Processing, Glasgow, Scotland, 1989. [S. Kiaei, J. Durgham]
65. "VLSI Design of Bit/Serial Adaptive IIR Filters," Proc. of IEEE Pacific Conference on Communications, Computers, and Signal Processing, Victoria, Canada, pp. 650-652, June 1989. [R. Badyal, S. Kiaei]
66. "CCA Approach for ARMA Spectral Analysis," Proc. of IEEE International Symposium on Circuits and Systems, Portland, OR, pp. 1319-1322, May 1989. [S. Kiaei, L. Luo]
67. "Canonical Correlation Analysis (CCA) for ARMA Spectral Estimation," IEEE International Symposium on Circuits and Systems, May, 1989. [Kiaei, S.; Luo, L.]
68. "VLSI Implementation of Adaptive Bit/Serial IIR Filters," IEEE Pacific Rim Conference on Communications, Computers and Signal Processing, June 1989. [Badyal, R.; Kiaei, S.]
69. "VLSI design of WAP for Recursive Equations," VLSI Signal Processing, 1988. [S. Kiaei, U. Desai]

70. "Independent Data Flow Wavefront Array Processors for Recursive Equations," Proc. of 20th Annual Conference on Information Sciences and Systems, Princeton University, NJ, 1986. [S. Kiaei, U. Desai]
71. "A Stochastic Realization Approach to Reduced-Order Hierarchical Estimation," Proc. of 24th IEEE Conference on Dec., Ft. Lauderdale, FL, pp. 416-421, December 1985. [U. Desai, S. Kiaei]
72. "Hierarchical Estimation Algorithms," Proc. of IEEE Conference on Man, Cybernetics, and Systems, Tucson, AZ, October 1985. [U. Desai S. Kiaei]
73. "Approximation of Markovian Models with Non-Constant Parameters," Proc. of 23rd IEEE Conference on Dec., Las Vegas, NV, pp. 1642-1644, December 1984. [U. Desai, S. Banerjee, S. Kiaei]
74. "A Canonical Correlation Approach to Reduced-Order LQR Design," Proc. of 23rd IEEE Conference on Dec., Las Vegas, NV, pp. 1523-1528, December 1984. [U. Desai, S. Banerjee, S. Kiaei]

** Note: In some of the above papers marked by *, the ordering/list of the co-author names may not be exact since I could not find the final copy of the paper in my folders.*

GRADUATE STUDENT ADVISEES & RESEARCH PROJECT

(Students graduated from Oregon State University, current employment to the best of my knowledge)

1. J. Durgam, VLSI Design of Dynamically Reconfigurable Array Processors, MSEE, 1988. Intel.
2. J. Gilbert, Minimization Techniques for PLAs, MSEE, 1988, Tektronix.
3. L. Luo, CCA Methods for ARMA Spectral Estimation, MSEE, 1989. Berkeley Research Center
4. E. Zahl, Enhancement Methods for A/D Noise Reduction, MSEE, 1989. AT&T
5. L. Aihua, Synthesis of MRAs, MSEE, 1990. Intel.
6. F. Aslam, Image Restoration Methods, MSEE, 1990.
7. S.H. Chee, FSCL Circuits for Mixed-Mode IC's, MSEE, 1990. Linear Tech.
8. C. Dawson, MSEE, 1990. Boeing
9. A. Chow, Source-Coupled Logic ALU, MSEE, 1990. Intel
10. S. Maskai, Decimation Filters Using FSCL Circuits, MSEE, 1991. Intel
11. L. Louis, VLSI Implementation of Toeplitz Matrices, MSEE, 1991.
12. R. Badyal, Bit/Serial VLSI Design of IIR Filters, MSEE, 1992, HP
13. Lap Mui, Piece-Wise Linear Schedule for VLSI Arrays, MSEE, 1992. HP
14. S. Abdennadher, Adaptive Sigma-Delta Modulators, MSEE, 1992. Level One
15. H. Bribech, Second Order Adaptive A/D Schemes, MSEE, 1992.
16. B. Hickman, MSEE, 92. Tektronix
17. M. Maleki, Current-Mode Flash A/D, MSEE, 1992. University of Oregon
18. Man Wong, Low-Noise Decimation Filter for Mixed-Mode ICs, MSEE, 1993, Motorola.
19. Anu Krishna Swamy, Low Noise IC Blocks for Mixed-mode IC's, MSEE, 1993, Ph.D., 1997.
20. Manu Srivastava, Comparison of Differential Logic (FSCL, CVSL, DSLL), MSEE, 1994, Intel.
21. Joel Oren, VLSI Design of Asynchronous FIR Filters, MSEE thesis, Feb. 1994. E-Systems.
22. Y. Zheng, VLSI Design and Synthesis of Multi-Rate Arrays, Ph.D. March 94, Hughes Research.
23. Satish Kulkarni, Low-Sensitivity Filters, MSEE, 1995, Motorola.
24. Amit Dutta, Multi-user Interference Cancellation, Ph.D, Dec. 97. AKM Design.
25. Dwight Poplin, Multiplierless MPEG Decoder, MSEE, 1996. HP.
26. Maxim Scarpa, Adaptive I/Q Miss-match Correction for Direct Conversion Receivers, MSEE 1998.

27. Jeff McNeal, Sigma-Delta Frequency-to-Time Conversion, MSEE, 1998. Level One Comm.
28. Julia Vogel, Adaptive DC offset Cancellation, MSEE, 1998.Germany.
29. Takao Inoue, MS, Echo Cancellation for ADSL, 1998. MSEE, The U of Texas at Austin.
30. Navid Lashkarian, Frequency off-set estimation and Synchronization of OFDM systems, Ph.D., June 1999. Centellium.
31. Guner Arslan, (co-advisor with B. Evans), "Fast Equalization for DMT systems, with applications to ADSL," Ph.D. from The University of Texas at Austin, 2000
32. Salem Abdennadher, I/Q Mismatch Correction for RF Wireless transceivers, Ph.D., Expected 2000/01 [Passed Qualifying & Prelim exam], Level One Comm/Intel.
33. Can Sandalci, DSL Line Driver, Ph.D., Expected 2000/01 [Passed Qualifying exam], Intel.

(Students graduated from Arizona State University, current employment to the best of my knowledge)

34. Dean Badillo, Low-Cost VCO Ring Oscillators, Intel, Chandler, Arizona State University
35. Hemanth Shivalingaiah, Multi-Band Low Noise Amplifiers, Ph.D. Student at Arizona State University
36. Siamak Abedinpour, Freescale, Tempe, Arizona
37. Shahin Farahani, Freescale, Tempe, Arizona
38. Nazanin Darbanian, Freescale, Tempe, Arizona

CURRENT GRADUATE STUDENTS:

- Jennifer Kitchen
Research Topic: Power Amplifier, Power Management
- Ilker Deligoz
Research Topic: Power Amplifier
- Marnie Wong
Research Topic: Power Management
- Umar Lyles
Research Topic: Power Management
- Shahin Mehdizad Taleie
Research Topic: MEMS

UNIVERSITY COMMITTEES

Various Committees at ASU

Oregon State University, University Graduate Student Admission Committee, 88-90

Oregon State University, Research Council, 90-91

Oregon State University, ECE Dept., Computer Engineering Section Leader, 89-91

Oregon State University, ECE Dept., Faculty Search Committee, 90-93, 96

Oregon State University, ECE Dept., Department Head Search Committee, 91/92

Oregon State University, ECE Department Promotion and Tenure Committee, 96

Oregon State University, Various other university and departmental committee 88-93.

INDUSTRY COMMITTEES

Arizona Telecommunications and Information Council (ATIC), Board Member

CAS Fellows Committee (ends December 31, 2006)

INSTRUCTIONAL SUMMARY

<u>YEAR</u>	<u>TERM</u>	<u>COURSE</u>	<u>Level</u>
1987, OSU	Fall	ECE 101 (1/2); ECE Orientation	Freshman
1988, OSU	Winter	ECE 478; Computer Architecture I	Senior/Graduate
	Spring	ECE 479; Computer Architecture II	Senior/Graduate
	Fall	ECE 579; VLSI Array Processing	Graduate
1989, OSU	Winter	ECE 518, VLSI System Design	Graduate
	Spring	ECE 563; Advance DSP	Graduate
	Fall	ECE 507A; Graduate Seminar	Graduate
1990, OSU OCATE, Tektronix OSU	Winter	ECE 322, Analog Electronic Circuits	Junior
	Spring	ECE 563; Advance DSP	Graduate
	Spring	ECE 563; Advance DSP,	Graduate
	Fall	ECE 679; VLSI Signal Processing	Graduate
1991, OSU	Winter	ECE 517; Digital Integrated Circuits	Graduate
	Spring	ECE 567; Advance DSP	Graduate
	Fall	ECE 679; VLSI Signal Processing	Graduate
1992, OSU OCATE, Tektronix	Winter	ECE 322; Analog Electronic Circuits	Junior
	Spring	ECE 323; Digital Electronics Circuits	Junior
	Spring	ECE 567; Advance DSP	Graduate
	Fall	ECE 516 ; Analog CMOS design	Graduate
	Fall	ECE 516, Advance Analog Design	Graduate

1993, OSU	Winter	ECE 322; Analog Electronic Circuits	Junior
	Spring	ECE 323; Digital Electronics Circuits	Junior
	Spring	ECE 567; Advance DSP	Graduate
1994 Motorola	Winter	Digital Audio Processing	Graduate
1996	Fall	ECE 669 Wireless Transceiver Design ECE 516 Analog CMOS Design	Graduate
1997	Winter	ECE 669 Wireless Comm. System ECE 464 Digital Signal Processing	Graduate Senior/Graduate
	Spring	ECE 574 VLSI System Design	Senior/Graduate
		ECE 567 Advance DSP	Graduate
1998/99	Fall	EE381k; Intro to Telecomm Systems	Senior/Graduate
UT Austin	Spring	EE381k-2; Digital Comm.	Graduate
2001, ASU	Spring	EEE 598; Wireless Transceiver Design	Graduate
2001/2002	Fall	EEE 524; Wireless Transceiver Design	Graduate
	Spring	EEE 433; Analog Integrated Circuits	Graduate
2002/2003	Fall	EEE 524; Wireless Transceiver Design	Graduate
	Spring	EEE 433; Analog Integrated Circuits	Graduate
2003/2004	Fall	EEE 524; Wireless Transceiver Design	Graduate
	Spring	EEE 433; Analog Integrated Circuits	Graduate
2004/2005	Fall	EEE 433; Analog Integrated Circuits	Graduate
	Spring	EEE 524; Wireless Transceiver Design	Graduate
2005/2006	Fall	EEE 433; Analog Integrated Circuits	Graduate
	Spring	EEE 524; Wireless Transceiver Design	Graduate