Position Paper: MEMS Packaging at the Wafer Level

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Various market surveys have predicted rapid commercial growth of MEMS. If the field of MEMS lives up to the expectations, it will dramatically improve and change various technology fronts. However, before laboratory-made, prototype devices can be transformed into commercial products, cost-effective packaging processes have to be established. Even in the making of a standard ic (integrated circuit), packaging process can take up to 95% of the total manufacturing cost. Issues in MEMS packaging are much more difficult to solve due to stringent requirements for handling, processing and protection of fragile microstructures.

Unlike regular ics, the diversity of MEMS complicates the packaging problems. For example, it has been suggested that MEMS packaging should be considered right from the beginning of the device development and manufacturing processes. Packaging schemes should be designed and incorporated into the device fabrication process to reduce the post-packaging costs. Each MEMS device may have its own specially designed packaging methods which are best fit to their particular functions. On the other hand, a versatile approach for MEMS packaging is attractive. Especially, many devices are now fabricated by integrating MEMS and microelectronics on the same chip.

There is a tremendous need for a versatile post-packaging process at the wafer-level for MEMS after foundry services are completed [1]. For example, in a MEMS accelerometer fabricated by analog devices inc. [2], the central sensor is a free-standing microstructure and it is desireable to protect this sensor during the packaging process. Moreover, it may be necessary for some MEMS devices to encapsulate the microstructures in vacuum environment for applications such as resonant accelerometers or gyroscopes [3,4]. Therefore, a versatile approach for wafer-level MEMS packaging must meet several goals. It should be insensitive to both MEMS structures and pre-fabricated microelectronics. It should be generally applicable to package devices fabricated by different processes for various applications. It should adopt the well-developed ic packaging technology to save research and development efforts.

The economic advantage of conducting wafer-level MEMS packaging is tremendous but it is very difficult to establish universal processes. In the MEMS packaging area, various approaches can be characterized in two categories: integrated process and wafer bonding process. Integrated process puts MEMS encapsulation as one of the goals of micromachining processes in a way that several extra steps, including deposition, patterning, etching are added to fabricate "micro shells" to protect MEMS structures. Typical examples are a reactive sealing method to seal vibratory micromachined beams [5]; an epitaxial silicon cap to seal microstructures [6]; a silicon nitride shell to seal mechanical resonator for wireless communication applications [7]; a new fabrication technology for embedding microstructures and CMOS circuitry [8]. Wafer bonding processes use fusion bonding, anodic bonding, eutectic bonding or solder bonding methods to encapsulate MEMS structures by using a second substrate of silicon, glass or other materials. Unfortunately, integrated processes suffer from the drawbacks of process-dependency, and not suitable for post-

processing. Wafer bonding processes suffer from the requirement of high temperature processing and flat surface for bonding. Therefore, there is currently no universal process for MEMS packaging at the wafer-level.

A unique approach of "*MEMS Post-Packaging by Localized Heating and Bonding*" is proposed. This process will package and protect the MEMS devices on the wafer-level by using "*localized heating and bonding",* The basic scheme is to fabricate a second "substrate cap" with properly designed micro cavity, microheater and bonding material as illustrated in Figure 1. This substrate is then bonded with the MEMS wafer by using localized heating and bonding. After this wafer-level *post-packaging* process, the wafer can be diced and the well-established chip-scale packaging technology in IC industry can follow to finish the final packaging processes. Initial work based on this approach has produced very promising results, including localized silicon-to-gold eutectic bonding [9], localized silicon-to-glass fusion bonding [10], localized indium solder bonding [11] and localized aluminum-to-glass bonding [12]. The continuation of this approach may lead to the universal MEMS post-packaging process.

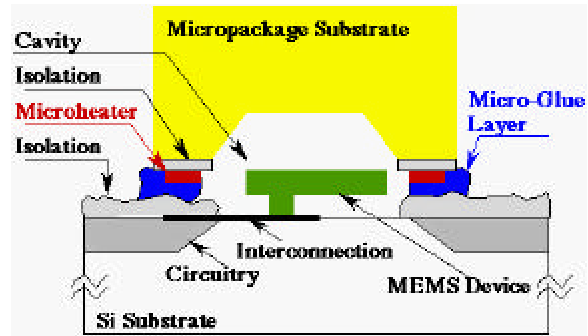

Fig.1, Schematic diagram of MEMS post-packaging by localized heating and bonding.

REFERENCES:

[1] T.A. Core, W.K. Tsang, and S. Sherman, "Fabrication Technology for an Integrated Surface-Micromachined Sensor", *Solid State Technology*, October, pp. 39-47, 1993.

[2] D. Koester, R. Majedevan, A. Shishkoff and K. Marcus, "Multi-User MEMS Processes (MUMPS) Introduction and Design Rules, rev. 4, MCNC MEMS Technology Applications Center, Research Triangle Park, NC 27709, July, 1996.

[3] D. Hicks, S.-C. Chang, M.W. Putty and D. S. Eddy, "Piezoelectrically Activated Resonant Bridge Microaccelerometer", *1994 Solid-State Sensors and Actuators Workshop*",225-228, 1994.

[4] M. Putty and K. Najafi, "A Micromachined Gyroscope", *1994 Solid-State Sensors and Actuators Workshop*",212-220, 1994.

[5] J.J. Sniegowski, H. Guckle and R.T. Christenson, "Performance Characteristics of Second Generation polysilicon Resonating Beam Force Transducers", *IEEE Solid-State Sensor and Actuator Workshop*, Hilton Head Island, 9-12, 1990.

[6] K. Ikeda, H. Kuwayama et al., "Silicon Pressure Sensor with Resonant Strain Gages Built into Diaphragm", *Digest of the 7th Sensor Symposium*, pp. 55-58, 1988.

[7] Liwei Lin, R.T. Howe and A.P. Pisano, "Microelectromechanical Filters for Signal Processing," *IEEE/ASME Journal of Microelectromechanical Systems*, Vol. 7, pp. 286-294, Sep. 1998..

[8] J. Smith, S. Montague, J. Sniegowski, R. Manginell, P. McWhorter, and R. Huber, "Characterization of the Embedded Micromechanical Device Approach to the Monolithic Integration of MEMS with CMOS", *SPIE* vol. 2879, Oct. 1996.

[9] Liwei Lin, Y.T. Cheng and K. Najafi, "Formation of Silicon-Gold Eutectic Bond Using Localized Heating Method," *Japanese Journal of Applied Physics, Part II*, Vol. 11B, pp. 1412-1414, Nov. 1998.

[10] Y.T. Cheng, Liwei Lin and Khalil Najafi, "Localized Silicon Fusion and Eutectic Bonding for MEMS Fabrication and Packaging," *IEEE/ASME Journal of Microelectromechanical Systems*, Vol. 9, pp. 3-8, March 2000.

[11] Yu-Ting Cheng, Liwei Lin and Khalil Najafi, "Localized Bonding with PSG or Indium Solder as Intermediate Layer," *Proceedings of IEEE Micro Electro Mechanical Systems Workshop*, pp. 285-289, Jan. 1999, Orlando, Florida.

[12] Y.T. Cheng, Liwei Lin and K. Najafi, "Fabrication and Hermeticity Testing of a Glass-Silicon Package Formed Using Localized Aluminum/Silicon-to-Glass Bonding," *Proceedings of IEEE Micro Electro Mechanical Systems Workshop*, pp. 757-762, Jan. 2000, Miyazaki, Japan.