

1. Introduction

1.1 Market Forces and the State of the Art

The most important factor driving continuous device improvement is the semiconductor industry's relentless effort to reduce the cost per function on a chip. The way this is done is to put more devices on a chip while either reducing manufacturing costs or holding them constant. This leads to three methods of reducing the cost per function. The first is transistor scaling, which involves reducing the transistor size in accordance with some goal, i.e. keeping the electric field constant from one generation to the next. With smaller transistors, more can fit into a given area than in the previous generation. The second method is circuit cleverness, which is associated with the physical layout of the transistors with respect to each other. If the transistors can be packed into a tighter space, then more devices can fit into a given area than before. The third method is to make the die larger. More devices can be fabricated on a larger die. All the while, the semiconductor industry is constantly looking for technological breakthroughs to decrease the manufacturing cost. All of this effort serves to reduce the cost per function on a chip.

Device engineers are most concerned with the method of transistor scaling introduced in the previous paragraph. There are some problems associated with device scaling, however. Critical dimensions, such as transistor gate length and oxide thickness, are reaching physical limitations. Considering the manufacturing issues, photolithography becomes difficult as the feature sizes approach the wavelength of ultraviolet light. In addition, it is difficult to control the oxide thickness when the oxide is made up of just a few monolayers. In addition to the processing issues there are also some fundamental device issues. As the oxide thickness becomes very thin, the gate leakage current due to tunneling increases dramatically. This significantly affects the power requirements of the chip and the oxide reliability. Short-channel effects (SCEs), such as drain-induced barrier lowering (DIBL) and the Early effect in bipolar junction transistors (BJT), degrade the device performance. Hot carriers also degrade device reliability.

One solution to the above-described problems is to implement devices using materials other than Si. Materials that have been proposed include silicon germanium ($\text{Si}_{1-x}\text{Ge}_x$) and carbon-doped silicon alloys. It has already been demonstrated experimentally, for example, that at $T=300\text{K}$, the effective hole enhancement of about 50% can be achieved using the SiGe technology.¹ Another alternative for achieving enhanced device performance is to use silicon-on-insulator (SOI) materials. Devices fabricated in this way are also found to be advantageous over their bulk silicon counterparts in terms of reduced parasitic capacitances, reduced leakage currents, increased radiation hardness, as well as less expensive fabrication processes.

1.1.1 Device Structures in $\text{Si}_{1-x}\text{Ge}_x$ Material Systems

A variety of devices utilizing $\text{Si}_{1-x}\text{Ge}_x$ has been studied, including the heterojunction bipolar transistor (HBT).^{2,3,4,5} There, the introduction of Ge into the base layer of an otherwise all-silicon bipolar transistor created a significant improvement in the operating frequency, current noise and power capabilities while maintaining the key advantages of a state-of-the-art BiCMOS process technology, including high integration level and economy of scale. Recent studies suggest that circuits fabricated in this technology are capable of fulfilling application requirements for RF analog in the 1-5 GHz range and for high-speed digital circuits at or above the 10 Gb/s range, with potentially lower power, lower cost and higher reliability when compared to other high-speed RF technology counterparts.⁶ Strained $\text{Si}_{1-x}\text{Ge}_x$ alloys were found to be very attractive for optoelectronics applications as well.⁷

However, up until now, electron transport has been studied mainly in surface or buried-channel strained-Si n -MOSFET devices.^{8,9,10,11,12,13,14} For these device structures, it was found that the curvature of the conduction bands of a strained-Si material systems does not significantly differ from pure Si, although the relative offset of the six conduction bands changes. As a result, when investigating the transport properties of strained-Si, one can use the well known Si effective masses and non-parabolicity factors for the case of moderate biasing conditions, i.e., when full-band effects and impact ionization are not dominating the device transport behavior. It was also shown that under high field conditions, the saturation drift velocity of strained-Si is almost the same as that of unstrained-Si and, as a result of this, there is little change in the electron transport properties of these novel device structures. In addition, the growth of the underlying relaxed $\text{Si}_{1-x}\text{Ge}_x$ buffer layer adds significant fabrication cost.

What has not been investigated so far are the transport properties of p -channel $\text{Si}_{1-x}\text{Ge}_x$ devices, schematically shown in Figure 1, that can be easily fabricated using slight modification of the existing Si processing. The enhanced hole mobility in these structures offers promise for enhanced device performance. Hence, it is ***Thrust one of this research proposal*** to investigate the transport properties of p -channel devices including the band structure effects. As part of an existing NSF proposal, we have shown that significant correction to the band structure of $\text{Si}_{1-x}\text{Ge}_x$ is observed in the valence bands. The spin-orbit splitting at the Γ -point is increased as the Ge concentration, x , is increased. Furthermore, strain splitting and band warpage also increase with increasing the Ge concentration. It is believed that this splitting and warpage will enhance low and high-field hole transport properties of

$\text{Si}_{1-x}\text{Ge}_x$ devices. Therefore, the implications for high-speed and high frequency device applications are expected to be significant.

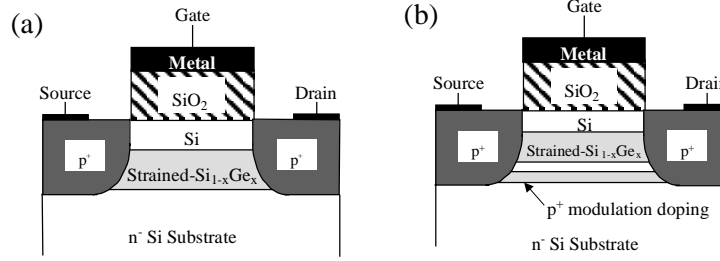


Figure 1. (a) p -MOSFET with a buried $\text{Si}_{1-x}\text{Ge}_x$ hole channel. (b) Modulation-doped p -MOSFET where the thin p -type doping supplies carriers to the $\text{Si}_{1-x}\text{Ge}_x$ channel layer, thus extending the voltage range over which transport is dominated by carriers in this higher mobility layer.

1.1.2 Device structures in SOI material system

Silicon on insulator (SOI) devices can be separated into two broad categories: partially-depleted (PD) and fully-depleted (FD) SOI devices. In a significant number of investigations, it has been shown that FD-SOI technology has the advantages over PD-SOI technology with regard to lower junction capacitance and better subthreshold swing¹⁵. However, the conventional fully depleted SOI MOSFET is known to have worse short-channel effects than bulk MOSFETs and partially depleted SOI MOSFETs¹⁶. It has been shown recently that the ultra-thin body (UTB) device structure, proposed by Choi *et al.*¹⁷ (schematically shown in Figure 2), eliminates the leakage paths between source and drain. Nearly all the leakage current at $V_G = 0$ V in the $T_{\text{Si}} = 7$ nm flows along the bottom 2 nm of the body, which is least strongly controlled by the gate. Therefore, by eliminating these 2 nm, i.e. making $T_{\text{Si}} = 5$ nm, one can reduce the leakage by 30 times in this device structure.

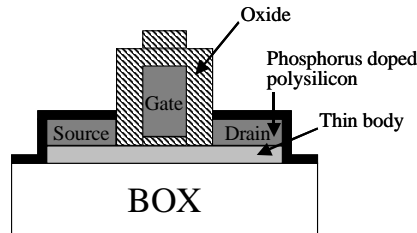


Figure 2. Schematic of an ultra-thin body SOI MOSFET.

It has also been shown that in both PD and FD-SOI devices there is a threshold voltage increase that depends upon both the impurity concentration and the SOI film thickness, because the inversion layer is very thin but as wide as normal gate electrodes. However, in an ultra-narrow SOI MOSFET, proposed by Majima *et al.*,¹⁸ and schematically shown in Figure 3, the threshold voltage not only depends on the SOI thickness but also on the channel width, because horizontal carrier confinement also takes place in the narrow channel. This channel width dependence of the threshold voltage on the quantum confinement is referred to as the quantum mechanical narrow channel effect.

Due to the experimental evidence of threshold voltage shift and the observation of Coulomb-blockade effects in the narrowest-width devices from Figure 3, it is **Thrust 2 of this research project** to investigate the current-voltage characteristics of narrow-width FD-SOI MOSFETs. For this purpose we will follow two different approaches. First, we will utilize the effective-potential approach, introduced in Section 1.3, combined with a Monte-Carlo particle based approach that we have developed as part of an existing NSF-CAREER project. The second path we will follow will use the self-consistent solutions of the 3D Poisson equation in conjunction with the transfer-matrix approach introduced in Section 4.2.3 of this research proposal.

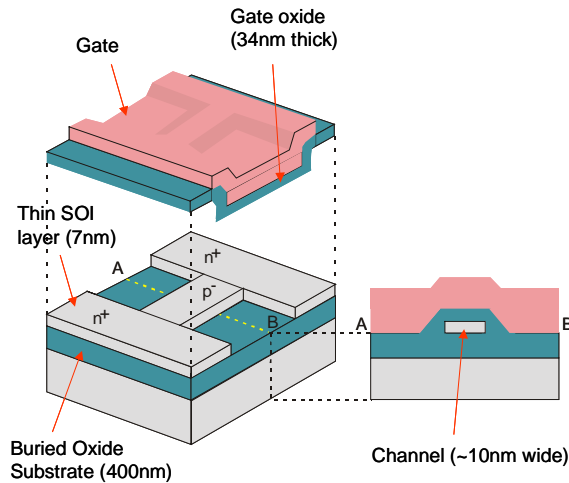


Figure 3. Device structure of ultra-narrow channel FD-SOI device structure. It consists of a thick silicon substrate, on top of which is grown 400 nm of buried oxide. The thickness of the silicon-on-insulator (SOI) layer is 7 nm, with p -region width between 7 and 15 nm. On top of the SOI layer sits gate-oxide layer, the thickness of which is 34 nm.

1.2 Device Simulation

The standard sequence that one follows when modeling device structures of interest includes a process simulation step, followed by a device simulation, and finalized with a circuit simulation step. In this regard, device simulation is the process of using computers to calculate the behavior of electronic devices, i.e. the current-voltage (I - V) curves of a device. The devices are defined mathematically in terms of their dimension, material composition, and other relevant physical information, all of which is obtained from the process simulation step.

It is also important to stress here that simulation is playing a key role in device development today. There are two issues that make simulation important. Product cycles are getting shorter with each generation, and the demand for production wafers overshadows development efforts in the factory. Consider the product cycle issue first. In order for companies to maintain their competitive edge, products have to be taken from design to production in less than 18 months. As a result, the development phase of the cycle is getting shorter. Contrast this requirement with the fact that it takes 2-3 months, depending on complexity, to run a wafer lot through a factory. The specifications for experiments run through the factory must be near the final form. While simulations may not be completely predictive, they provide a good initial guess. This can ultimately reduce the number of iterations during the device development phase.

The second issue that reinforces the need for simulation is the production pressures that factories face. In order to meet customer demand, development factories are giving way to production space. It is also expensive to run experiments through a production facility. The resources could have otherwise been used to produce sellable products. Again, device simulation can be used to decrease the number of experiments run through a factory. Device simulation can be used as a tool to guide manufacturing down the right path, thereby decreasing the development time and costs.

Contrary to the recent technological advances, present state of the art in device simulation is currently lacking in the ability to treat the new challenges in scaling of device dimensions from conventional devices down to quantum scale devices. For silicon devices with active regions below 0.1 microns in diameter, macroscopic transport descriptions based on drift-diffusion models are clearly inadequate. Even standard hydrodynamic models do not provide a sufficiently accurate description since they neglect significant contributions from the tail of the phase space distribution function in the channel regions.^{19,20} Within the requirements of self-consistently solving the coupled transport-field problem, there are several computational challenges as well. One is the necessity to solve both the transport and the Poisson's equations over the full 3D domain of the device. As a result, highly efficient algorithms targeted to high-end computational platforms are required to fully solve even the appropriate field problems.

The appropriate level of approximation necessary to capture the proper non-equilibrium transport physics relevant to a future device model is an even more challenging problem both computationally and from a fundamental physics framework. It is now common practice in industry to use either drift-diffusion or standard hydrodynamic models in trying to understand the operation of as-fabricated devices, by adjusting any number of phenomenological parameters (e.g. mobility, impact ionization coefficient, etc.). However, such tools do not have predictive capability for ultra-small structures, for which it is necessary to relax some of the approximations in the Boltzmann

transport equation. Therefore, it becomes imperative to start using some of the quantum transport approaches, including the Green's function technique and the Landauer scattering matrix theory. The PI of this research proposal has significant experience in both areas. Namely, the PI has worked for several years on the low-field mobility calculation using Greens functions technique for a variety of material systems.^{21,22,23} She has also performed quantum transport calculations based on the transfer matrix approach.²⁴ The existence of an in-house simulation tool based on the transfer matrix approach, that is discussed in more details in Section 4.2.3, will significantly alleviate the effort needed in some of the proposed research activities. Only minor modification of this tool will be needed for modeling, for example, the SOI device structures.

1.3 Quantum and Effective Potentials for Device Modeling

Due to the complexity of dealing with quantum transport approaches, and the desire to have device simulation tools which are able to deal with multiple levels of length scales and complexity, from the quantum regime down to the classical regime, increasing interest is being focused on the use of quantum mechanically derived potentials that may be added as "corrections" to semi-classical simulation tools. The idea of quantum potentials derives from the hydrodynamic formulation of quantum mechanics first introduced by de Broglie and Madelung,^{25,26,27} and later developed by Bohm.^{28,29} In this picture, the wave function is written in complex form in terms of its amplitude and phase, $\psi(\mathbf{r}, t) = R(\mathbf{r}, t) \exp[iS(\mathbf{r}, t)/\hbar]$, and when substituted back into the Schrödinger equation it leads to coupled equations of motion for the density and phase, of the form

$$\frac{\partial \rho(\mathbf{r}, t)}{\partial t} + \nabla \cdot \left(\rho \frac{1}{m} \nabla S \right) = 0, \quad (1)$$

$$-\frac{\partial S(\mathbf{r}, t)}{\partial t} = \frac{1}{2m} (\nabla S)^2 + V(\mathbf{r}, t) + Q(\rho, \mathbf{r}, t), \quad (2)$$

where the probability density is $\rho(\mathbf{r}, t) = R(\mathbf{r}, t)^2$. With identification of the velocity as $\mathbf{v} = \nabla S / m$, and the flux as $\mathbf{j} = \rho \mathbf{v}$, equation (1) is the continuity equation. Hence, equations (1) and (2), arising from this so called Madelung transformation to the Schrödinger equation, have the form of classical hydrodynamic equations with the addition of an extra potential, often referred to as the *quantum* or *Bohm* potential, written as

$$Q = -\frac{\hbar^2}{2mR} \nabla^2 R \rightarrow -\frac{\hbar^2}{2m\sqrt{n}} \frac{\partial^2 \sqrt{n}}{\partial x^2}, \quad (3)$$

where the square root of the density n , represents the magnitude of the wave function R . The Bohm potential essentially represents a field through which the particle interacts with itself. It has been used, for example, in the study of wave packet tunneling through barriers,³⁰ where the effect of the quantum potential is seen to lower or smooth barriers, and hence allows particles to leak through.

An alternate form of the quantum potential was derived by Iafate *et al.*³¹ that arises from taking moments of the Wigner-Boltzmann equation, the kinetic equation describing the time evolution of the Wigner distribution function.³² This later quantum potential takes the form

$$V_Q = -\frac{\hbar^2}{8m} \frac{\partial^2 (\ln n)}{\partial x^2}, \quad (4)$$

and is sometimes referred to as the Wigner potential, or as the density gradient correction. Zhou *et al.*³³ derived a form for a smooth quantum potential based on the effective classical partition function of Feynman and Kleinert.³⁴ More recently, Gardner and Ringhofer derived a smooth quantum potential for hydrodynamic modeling valid to all orders of \hbar^2 , which involves a smoothing integration of the classical potential over space and temperature.³⁵

A standard way to include quantum effects into classical simulation tools is to add the above-described quantum potentials to the mean-field potential computed from solving the Poisson's equation. Such potential corrections have been employed mostly in the context of fluid approximations leading to the so-called quantum-hydrodynamic (QHD) equations.³⁶ The Bohm potential of Equation (3) has also been used in quantum particle-based simulations for quantum molecular dynamics calculations in quantum chemistry.³⁷ Again, the result differs from the classical molecular dynamics picture only by an additional quantum force term arising from the Bohm potential. These potential terms lead to tremendous problems for particle simulators since they involve higher derivatives of the electron density, which are almost impossible to compute from particle based methods due to statistical fluctuations. Moreover, for thermalized systems, their derivation relies on small potential variations and therefore these approximations are not valid close to barriers where they are actually needed most.

Analogous to the smoothed potential representations discussed for the QHD model above, it is desirable to define a smooth quantum potential for use in quantum particle based simulation. Ferry³⁸ suggested an *effective potential* that is derived from a wave packet description of particle motion, where the extent of the wave packet is de-

efined from the range of wavevectors established by the thermalized distribution function (characterized by an electron temperature). The effective potential seen by electrons is given by

$$V_{eff}(x) = \frac{1}{\sqrt{2\pi}a_0} \int_{-\infty}^{\infty} V(x') \exp\left(-\frac{(x-x')^2}{2a_0^2}\right) dx', \quad (5)$$

where $V(x')$ is the actual potential, and a_0 is the spatial spread of the wavepacket. The effective potential accounts for the *size of the electron* and its associated wavepacket, which feels the presence of barriers, etc. at a distance. From this *Ansatz*, the actual particle is treated as point-like in the presence of the effective potential associated with its wave-like nature, leading back to a classical particle simulation scheme. Some representative simulation results, which utilize this effective potential approach, are shown in Figure 4, where we plot the transfer and output characteristics of a 250 nm asymmetric n -channel MOSFET.^{39,40} We find that the quantum-mechanical space-quantization effects lead to threshold voltage shift of about 150 mV and drain current reduction between 30 and 40 %, depending upon the gate bias.

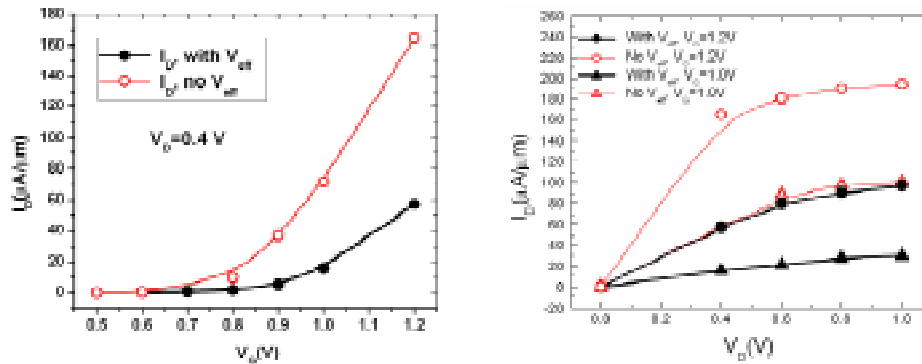


Figure 4. Left panel: transfer characteristics of a FIBMOS device. Right panel: device output characteristics.

The initial success with the effective potential approach, regarding accurate description of quantum-mechanical space-quantization effects in regular n -channel MOSFETs⁴¹ and in asymmetric n -channel MOS devices,³⁹ has encouraged the PI of this project to apply it to tunneling phenomena through thin oxides. The latter constitutes *Thrust three of this research project*. In addition, the applicability of other forms of effective potentials, such as the one proposed by Gardner and Ringhofer³⁵, will also be investigated as part of this research project.

2. Results of Prior NSF Support

2.1 Grant No. ECS-9802596

National Center for Computational Electronics

D. K. Ferry, S. M. Goodnick and D. Vasileska

\$265,000 (including 1 REU Student) 10/1/98-9/30/01

The research activity at ASU, performed as part of Descartes, can be separated into two major categories, particle-based and quantum transport simulations. In the case of particle-based simulations, we have addressed the following issues. (1) Proper inclusion of the short-range Coulomb interactions, and how they influence device output characteristics. (2) Use of the Full Band CA/Monte Carlo hybrid, which implements the CA method in regions of momentum space where most of the scattering events occur, and the MC method elsewhere, thus optimizing the relationship between memory and speed. (3) Development of efficient 3D Poisson equation solvers for 3D particle-based simulations. With respect to quantum transport calculations, we have performed self-consistent calculations for the spatial electron densities in quantum dots using a coupled recursive Green's function and a 2D Poisson solver. As part of the educational activities of this proposal, we have developed and installed on PUNCH a 1D Schrödinger-Poisson solver (SCHRED). The tool is currently residing on the Purdue Semiconductor Simulation Hub (PUNCH) (<http://www.ecn.purdue.edu/labs/punch>).

Publications Under Grant No. ECS-9802596

Journal Publications and Conference Proceedings

1. D. K. Ferry, R. A. Akis, D. P. Pivin, Jr., J. P. Bird, N. Holmberg, F. Badrieh, and D. Vasileska, "Quantum Transport in Ballistic Quantum Dots", *Physica E*, Vol. 3, pp. 137-144 (1998).

2. D. K. Ferry and J. R. Barker, "Issues in General Quantum Transport with Complex Potentials", *Applied Physics Letters*, Vol. 74, pp. 582-4 (1999).
3. D. Vasileska, and D. K. Ferry, "The influence of poly-silicon gates on the threshold voltage, inversion layer and total gate capacitance in scaled Si-MOSFETs", *Nanotechnology*, Vol. 10, pp.192-197 (1999).
4. W. J. Gross, D. Vasileska and D. K. Ferry, "A Novel Approach for Introducing the Electron-Electron and Electron-Impurity Interactions in Particle-Based Simulations", *IEEE Electron Device Lett.*, Vol. 20, No. 9, pp. 463-465 (1999).
5. (*invited paper*) D. Vasileska, W. J. Gross and D. K. Ferry, "Modeling of Deep-Submicrometer MOSFETs: Random impurity effects, threshold voltage shifts and gate capacitance attenuation", in *Proceedings of the 1998 Sixth International Workshop on Computational Electronics*, pp. 259-262 (1998).
6. R. Akis, D. Vasileska, and D.K. Ferry, "An overview of the 3D simulation efforts at Arizona State University-Understanding transport in quantum dots and the ultra-small devices of the future", in *Technical Proceedings of MSM99*, pp. 384-387 (1999).
7. F. Assad, Z. Ren, D. Vasileska, S. Datta and M. Lundstrom, "Modeling on-currents for *n*-MOSFETs: Ultimate limits vs. the NTRS", in *Technical Proceedings of MSM99*, pp. 388-390 (1999).
8. F. Assad, Z. Ren, D. Vasileska, S. Datta, and M. Lundstrom, "On the performance limits for Si MOSFETs: A theoretical study", *IEEE Trans. Electron Devices*, Vol. 47, No. 1, pp. 232-240 (2000).
9. M. Saraniti, S. J. Wigger, and S. M. Goodnick, "Full-Band Cellular Automata for Modeling Transport in Sub-Micrometer Devices", in *Proceedings of the 2nd International Conference on Modeling and Simulation of Microsystems* (Computational Publications, Boston) 380-383 (1999).
10. S. J. Wigger, M. Saraniti, and S. M. Goodnick, "Three-Dimensional Multi-Grid Poisson Solver for Modeling Semiconductor Devices", in *Proceedings of the 2nd International Conference on Modeling and Simulation of Microsystems* (Computational Publications, Boston) 415-418 (1999).
11. (*invited book chapter*) D. Vasileska, G. F. Formicone and D. K. Ferry, "Electron transport in surface-channel strained-Si MOSFETs and modulation-doped FETs", *to be published by Gordon and Breach*.
12. (*invited paper*) D. Vasileska, "Scaled Si-MOSFETs: The influence of space-quantization effects and poly-gate depletion on the threshold voltage, inversion layer and total gate capacitances," *Special Issue of the IEEE JMSM*, in press.
13. R. Akis and D. Vasileska, "Modeling artificial molecules composed of coupled quantum dots", in *Technical proceedings of MSM2000*.
14. W. J. Gross, D. Vasileska and D. K. Ferry, "3D Simulations of Ultra-Small MOSFETs with Real-Space Treatment of the Electron-Electron and Electron-Ion Interactions", *VLSI Design*, Vol. 10, pp. 437-452 (2000).
15. D. Vasileska, W. J. Gross, and D. K. Ferry, "Monte-Carlo particle-based simulations of deep-submicron *n*-MOSFETs with real-space treatment of electron-electron and electron-impurity interactions", *Superlattices and Microstructures*, Vol. 27, No. 2/3, pp. 147-157 (2000).
16. W. J. Gross, D. Vasileska and D. K. Ferry, "Ultra-small MOSFETs: The importance of the full Coulomb interaction on device characteristics", *IEEE Trans. Electron Devices*, Vol. 47, No. 10, pp. 1831-1837 (2000).
17. M. Houry, A. Gunther, S. Miličić, M. J. Rack, S. M. Goodnick, D. Vasileska, T. J. Thornton, and D. K. Ferry, "Single-electron quantum dots in silicon MOS structures", *Applied Physics A*, vol. 71, pp. 415-421 (2000).
18. D. K. Ferry, R. Akis, and D. Vasileska, "Quantum Effects in MOSFETs: Use of an Effective Potential in 3D Monte Carlo Simulation of Ultra-Short Channel Devices", *IEDM Tech. Dig.* (IEEE Press, New York, 2000) pp. 287-290.
19. R. Akis, L. Shifren, D. K. Ferry and D. Vasileska, "The effective potential and its use in simulation", *Phys. Stat. Sol. (b)*, Vol. 226, No. 1, pp. 1-8 (2001).
20. G. Speyer, D. Vasileska, and S. M. Goodnick, "Efficient Poisson equation solvers for large scale 3D simulations", *Proceedings of the 4th International Conference on Modeling and Simulation of Microsystems*, Hilton Head Island, SC, March 19-21, 2001.

Conference Presentations

1. (*invited talk*) D. Vasileska, W. J. Gross and D. K. Ferry, "Modeling of Deep-Submicrometer MOSFETs: Random impurity effects, threshold voltage shifts and gate capacitance attenuation", *1998 Sixth International Workshop on Computational Electronics*, Osaka, Japan.
2. (*invited talk*) Dragica Vasileska, "Discrete impurity effects in ultra-small devices of the future", *Nanotransistors: Technology, Physics, and simulation*, NIST Gaithersburg, February 8-9, 1999.
3. D. Vasileska, W. J. Gross and David K. Ferry, "Real-Space Treatment of Electron-Electron and Electron-Impurity Interactions in Monte Carlo Particle-Based Simulators", *APS March Meeting*, Atlanta, GA, March 1999.
4. M. Saraniti, S. J. Wigger, and S. M. Goodnick, "Full-Band Cellular Automata for Modeling Transport in Sub-Micrometer Devices", Presented at the *2nd International Conference on Modeling and Simulation of Microsystems*, San Juan, Puerto Rico, April 19-21st, 1999.
5. S. J. Wigger, M. Saraniti, and S. M. Goodnick, "Three-Dimensional Multi-Grid Poisson Solver for Modeling Semiconductor Devices", Presented at the *2nd International Conference on Modeling and Simulation of Microsystems*, San Juan, Puerto Rico, April 19-21st, 1999.
6. (*invited talk*) D. K. Ferry, "Effective Size of the Electron Wave Packet and its Role in Device Modeling", *3rd NASA Workshop on Device Modeling*, Moffett Field, CA, August 26-27, 1999.
7. (*invited talk*) D. Vasileska, "Monte Carlo particle-based simulations of deep-submicron *n*-MOSFETs with real-space treatment of electron-electron and electron-impurity interactions", *3rd NASA Workshop on Device Modeling*, Moffett Field, CA, August 26-27, 1999.
8. F. Badrieh, R. Akis, and D. K. Ferry, "Temperature Dependent Conductance in Single and Multiple Quantum Dots: The Role of Disorder", *Surfaces and Interfaces of Mesoscopic Devices*, Maui, December 1999.

9. F. Badrieh and D. K. Ferry, "Effect of Boundary Conditions on Quantum Anti-Dots in Presence of Magnetic Field", *Surfaces and Interfaces of Mesoscopic Devices*, Maui, December 1999.

2.2 Grant No. ECS-9875051

CAREER: Computation as a Means of Understanding the Operation of the Devices of the Future

D. Vasileska

\$205,000 (including 1 REU Student) 1/4/99-3/31/03

The 3D particle-based simulator, developed as part of this research project, utilizes analytical band structure and a Molecular Dynamics routine. The latter allowed us to properly account for the multi-ion contributions and local distortions in the scattering potential due to the movement of the free charges and carrier-density fluctuations. The simulator was used in the investigation of fluctuations in the threshold voltage and the on-state current due to discrete impurity effects in ultra-small MOSFETs. Local/non-local empirical pseudopotential code was also developed and used in the calculation of the energy band structure of strained-SiGe bulk material system. To be able to study transport in quantum dot structures, a 3D Schrödinger-Poisson solver was developed. It was used in the calculations of the energy level structure in Si quantum dots, fabricated within the Nanostructures Research Group at Arizona State University. The already completed REU student project involved development of a Monte Carlo code for GaAs material systems. Three Masters students graduated as part of this research project: Salvador Gonzalez, Gil Speyer and Srdjan Milicic. One Ph.D. student (William J. Gross) graduated while being partially supported from this research grant. One more graduate student is completing his Master's Degree by the end of the next year and continuing for a Ph.D.

Publications Under Grant No. ECS - 9875051

Journal Publications, Conference Proceedings and Book Chapters

1. W. J. Gross, D. Vasileska and D. K. Ferry, "A Novel Approach for Introducing the Electron-Electron and Electron-Impurity Interactions in Particle-Based Simulations", *IEEE Electron Device Lett.* 20, No. 9, pp.463-465 (1999).
2. W. J. Gross, D. Vasileska and D. K. Ferry, "3D Simulations of Ultra-Small MOSFETs with Real-Space Treatment of the Electron-Electron and Electron-Ion Interactions", *VLSI Design*, Vol. 10, pp. 437-452 (2000).
3. D. Vasileska, W. J. Gross, and D. K. Ferry, "Monte-Carlo particle-based simulations of deep-submicron *n*-MOSFETs with real-space treatment of electron-electron and electron-impurity interactions", *Superlattices and Microstructures*, Vol. 27, No. 2/3, pp. 147-157 (2000).
4. W. J. Gross, D. Vasileska and D. K. Ferry, "Ultra-small MOSFETs: The importance of the full Coulomb interaction on device characteristics", *IEEE Trans. Electron Devices*, Vol. 47, No. 10, pp. 1831-1837 (2000).
5. S. N. Miličić, R. Akis, D. Vasileska, A. Gunther and S. M. Goodnick, "3D Modeling of Discrete Impurity Effects in Silicon Quantum Dots: Energy Level Spacing and Scarring Effects", *Superlattices and Microstructures*, Vol. 28, No. 5/6, pp. 461-467 (2000).
6. M. Houry, A. Gunther, S. Miličić, M. J. Rack, S. M. Goodnick, D. Vasileska, T. J. Thornton, and D. K. Ferry, "Single-electron quantum dots in silicon MOS structures", *Applied Physics A*, vol. 71, pp. 415-421 (2000).
7. S. N. Miličić, R. Akis, D. Vasileska, A. Gunther and S. M. Goodnick, "3D Modeling of Discrete Impurity Effects in Silicon Quantum Dots: Energy Level Spacing and Scarring Effects", *Superlattices and Microstructures*, Vol. 28, No. 5/6, pp. 461-467 (2000).
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13. R. Akis, S. Milicic, D. K. Ferry, and D. Vasileska, "An effective potential method for including quantum effects into the simulation of ultra-short and ultra-narrow channel MOSFETs", *Proceedings of the 4th International Conference on Modeling and Simulation of Microsystems*, Hilton Head Island, SC, March 19-21, 2001, pp. 550-3.

Invited Presentations

1. "Real-Space Treatment of Electron-Electron and Electron-Impurity Interactions in Monte Carlo Particle-Based Simulators", *APS March Meeting*, Atlanta, GA, March 1999.
2. "Monte Carlo particle-based simulations of deep-submicron *n*-MOSFETs with real-space treatment of electron-electron and electron-impurity interactions", *3rd NASA Workshop on Device Modeling*, Moffett Field, CA, August 26-27, 1999.

3. "Discrete impurity effects in ultra-small MOSFETs", Workshop on Computational Materials and Electronics, Motorola, November 4th, 1999.
4. "Scaling limits of devices and modeling", A Workshop on Challenges in Advanced Electronic Device Simulation, September 5th, 2000, Seattle, Washington.
5. "Prospects/Challenges in modeling of ultra-small MOSFETs, quantum dots and SETs", Workshop entitled: *Challenges in Advanced Electronic Device Simulation*, Seattle, September 5th, 2000.
6. "The influence of quantum-mechanical space-quantization effect on 50 nm MOSFET operation", Second Annual Motorola Phoenix Workshop on Computational Materials Science and Electronics, Tempe, November 9-10, 2000.
7. "Effective potentials for quantum effects in MOSFETs", Maratea, Italy, June 2001, presentation given by Richard Akis.
8. "The Role of the Quantization Effects on the Operation of Ultrasmall MOSFETs, FIBMOS Devices and the SOI Device Structure", Motorola Workshop on Computational Materials and Electronics, November 12-14, 2001, Mesa, AZ.
9. "Empirical pseudopotential method for the band-structure calculation of strained-silicon germanium materials", Motorola Workshop on Computational Materials and Electronics, November 12-14, 2001, Mesa, AZ.

Student Presentations

1. S. Gonzalez, D. Vasileska, and A. A. Demkov, "Empirical pseudopotential method for the band structure calculation of strained $\text{Si}_{1-x}\text{Ge}_x$ materials", *IWCE-8*, Beckman Institute, University of Illinois at Urbana Champaign, October 15-17, 2001.
2. G. Speyer and D. Vasileska, "Multi-grid and Bi-CGSTAB solvers for large 3D systems", *IWCE-8*, Beckman Institute, University of Illinois at Urbana Champaign, October 15-17, 2001.
3. D. Vasileska, X. He, I. Knezevic and D. K. Schroder, "The role of quantum confinement on the operation of FIBMOS device", *IWCE-8*, Beckman Institute, University of Illinois at Urbana Champaign, October 15-17, 2001.
4. I. Knezevic, D. Vasileska, R. Akis, J. Kang, X. He, and D. K. Schroder, "Monte Carlo particle-based simulation of FIBMOS: Impact of strong quantum confinement and asymmetric channel doping on device performance and hot carrier reliability", *12th International Conference on Nonequilibrium Carrier Dynamics in Semiconductors (HCIS-12)*, Santa Fe, New Mexico, August 27-31, 2001.
5. I. Knezevic, D. Vasileska, R. Akis, J. Kang, X. He, and D. K. Schroder, "Monte Carlo particle-based simulations of FIBMOS devices", presented at the *4th International Conference on Modeling and Simulation of Microsystems*, Hilton Head Island, SC, March 19-21, 2001.
6. R. Akis, S. N. Milicic, D. K. Ferry, and D. Vasileska, "An effective potential method for including quantum effects into the simulation of ultra-short and ultra-narrow channel MOSFETs", presented at the *4th International Conference on Modeling and Simulation of Microsystems*, Hilton Head Island, SC, March 19-21, 2001.
7. D. K. Ferry, R. Akis, and D. Vasileska, "Quantum effects in MOSFETs: Use of an effective potential in 3D Monte Carlo simulation of ultra-short channel devices", *2000 IEEE International Electron Devices Meeting*, San Francisco, CA, December 11-13, 2000.
8. W. J. Gross, D. Vasileska and D. K. Ferry, "3D simulation of ultra-small MOSFETs: The role of discrete impurities on the device terminal characteristics", *7th International Workshop of Computational Electronics*, Glasgow, UK, May 21-25, 2000.
9. W. J. Gross, D. Vasileska, and D. K. Ferry, "Ultra-small MOSFETs: The importance of the full Coulomb interaction on device characteristics", *7th International Workshop of Computational Electronics*, Glasgow, UK, May 21-25, 2000.
10. J. Kang, X. He, D. Vasileska, and D. K. Schroder, "Optimization of FIBMOS through 2D Device Simulation", *7th International Workshop of Computational Electronics*, Glasgow, UK, May 21-25, 2000.
11. S. Gonzalez, D. Vasileska, and A. A. Demkov, "Empirical pseudopotential method for the band structure calculation of strained $\text{Si}_{1-x}\text{Ge}_x$ materials", *APS March Meeting* (12-16 of March), Seattle, 2000.
12. R. Akis, L. Shifren, D. Vasileska, and D. K. Ferry, "The effective potential: Incorporating quantum effects in classical device modeling", *4th International Workshop on Quantum Functional Devices*, Kanazawa, Japan, November 15-17, 2000, pp. 119-120.
13. S. N. Miličić, R. Akis, D. K. Ferry and D. Vasileska, "An effective potential method in simulation of SOI MOSFET structure", *Second Annual Motorola Phoenix Workshop on Computational Materials Science and Electronics*, Tempe, November 9-10, 2000. (poster).

3. Research Goals

The goals of the present research proposal are to develop a set of numerical tools for modeling p -channel strained $\text{Si}_x\text{Ge}_{1-x}$ MOSFETs and narrow-width SOI devices. A hierarchical approach will be pursued beginning at the Boltzmann equation level and going down the hierarchy of approximations towards full quantum transport modeling. Experimental calibration of these novel technologies will be done in collaboration with the Nanostructures Research Group at Arizona State University, and the local Industry including Motorola and Intel. Specific goals, which will be pursued as part of this research project, include:

- Development of a full-band Monte Carlo particle-based simulator for modeling p -channel strained $\text{Si}_x\text{Ge}_{1-x}$ MOSFETs including quantum corrections.
- Development of a Monte-Carlo-effective potential approach for modeling ultra-small MOSFETs and narrow-width FD-SOI devices.
- Development of quantum transport simulator for modeling narrow channel SOI devices and single-electron transistors in the narrowest channel SOI devices.

4. Research Approach

4.1 Semi-Classical Boltzmann Approach to Modeling of $\text{Si}_x\text{Ge}_{1-x}$ Devices

4.1.1 Full Band Monte Carlo

Under the current NSF grant we have developed a 2D/3D Monte Carlo particle-based simulator coupled with a 2D/3D Poisson equation solver. A full-band model based on the empirical pseudopotential method (EPM), in which spin-orbit interaction is included using the Löwdin⁴² quasi-degenerate perturbation theory, was also developed as part of the NSF-CAREER and an ongoing ONR project. The basic idea behind Löwdin quasi-degenerate perturbation theory is to divide the states in the initial matrix (of size N) into two classes. The first class (class A) consists of low energy states that are treated exactly. The second class (class B), on the other hand, includes high energy states that are treated perturbatively. Löwdin used the variational principle to arrive at a perturbation formula, which gives the influence of the higher-lying states on the lower-lying states. The benefits of using the quasi-degenerate perturbation theory due to Löwdin are the following ones:

- (a) One does not need to solve an eigenvalue problem of size $2N$ when spin is included in the problem.
- (b) Degenerate and non-degenerate states are treated on an equal footing, which means that there is no need to first lift the degeneracy of the states by finding linear combinations of the zeroth-order degenerate states, and then apply the standard perturbative approach. Within this scheme, the degeneracy of the states is lifted via the introduction of an effective matrix element. Simplifications to the conventional degenerate perturbation theory have been worked out by Van Vleck⁴³.

With regard to the choice of the EPM coupling parameters, the bulk silicon germanium alloy was treated using the virtual crystal approximation, i.e., a linear interpolation of the EPM parameters. Strain was incorporated into the model by applying a strain tensor, which was derived from basic elastic theory, to the reciprocal lattice vectors. Finally, the density of states for both holes and electrons was calculated using a numerical integration technique due to Gilat and Raubenheimer.⁴⁴

However, the above-described method is suitable for modeling bulk materials only. For the case of heterostructures, as it occurs in p -channel SiGe devices, further modifications are needed. The reason for this is the following: The electronic states with mean-free path comparable to or longer than the well width are significantly influenced by the spatial modulation of the heterostructure. States with mean-free paths much less than the heterostructure period are kinetically confined within a particular material and are, thus, not much modified with respect to their bulk counterparts. As a result, electronic states close to the conduction or valence-band edges will be the ones that are modified most. Since carriers near the source region of the device occupy precisely those states, for proper transport calculations it is mandatory to take these modifications into account.

To accomplish this task, we will follow the approach due to Smith and Mailhot.^{45,46} Namely, we will utilize our empirical EPM code, developed as part of the ongoing NSF-CAREER project, to provide a basis set for the zone-center Bloch states using averaged pseudopotential form factors. As we have done previously, by including spin, eight zone-center Bloch states will be treated explicitly, and a large number of additional states will be included in Löwdin⁴² quasi-degenerate perturbation theory. The perturbation interaction will comprise the $\mathbf{k}\cdot\mathbf{p}$ term and ΔV term that equals the difference between the given material and the averaged pseudopotential. Perturbation theory will be applied to first order for the wavefunctions and to second order for the energies. The spin-orbit interaction and the stress interaction, due to possible lattice mismatch, will be taken between the explicitly included states. Using this description, Bloch and evanescent states will be found by solving a non-Hermitian eigenvalue problem. The states in the two materials will be joined at the interface using results derived about the normal component of the current-density operator.⁴⁵ This interface description will ensure flux conservation through the order in perturbation theory at which wavefunctions are calculated.

Besides the development of a $\mathbf{k}\cdot\mathbf{p}$ band structure code, *quantum corrections* to the semi-classical Monte Carlo algorithm will also be investigated as part of the proposed program of research. These include high-field effects such as collisional broadening and the intercollisional field effect,⁴⁷ for which various proposals exist for implementation in particle based simulators. In addition, we propose to add quantum mechanical tunneling in a treatment similar to that used in single electron device simulators. In a tunneling Hamiltonian approach, tunneling is treated as a scattering process, and hence may be tabulated for particles incident on potential barriers. These barriers include the oxide barrier for gate tunneling, as well as source-drain tunneling in MOS devices. It may further include tunneling in localized regions formed by discrete impurity fluctuations. A further problem that will be investigated in extending the existing particle-based approach, is how to include quantum mechanical phase in the free flight trajectories of the particles. An unambiguous construction of *quantum* trajectories, associated with pure states (in both configuration space and phase space) is provided by the Bohm-de Broglie *interpretation* of quantum mechanics.⁴⁸ Here, the Schrödinger equation for a carrier describes the deterministic, causal evolution of a

complex field, but is augmented by the postulate that the carrier may be considered as a classical point particle with position vector $\mathbf{x}(t)$ and momentum vector $\mathbf{p}(t)$ embedded within the pilot field $\psi(\mathbf{r},t)$. Proposals on modifying this approach to trajectory based simulation in semiconductors have been discussed and will be further investigated in the proposed project, as a method of incorporating quantum interference in conventional particle simulators.

The full-band Monte Carlo code will be coupled with multiprocessor field solvers to provide full 3D device modeling capability. The target device technology will revolve around scaled $\text{Si}_{1-x}\text{Ge}_x$ -MOSFET, such as short-channel strained $\text{Si}_x\text{Ge}_{1-x}$ MOSFETs. Calibration of such codes in practical geometries will be performed in collaboration with local groups at Motorola and Intel. Such calibration will utilize present process simulation tools available commercially to us together with process information on particular technologies to establish the proper device structure. Comparison with conventional (commercial) hydrodynamic and drift diffusion based simulators on the same structures will be made, and calibration of these tools with the full-band Monte Carlo will be performed.

4.2 Quantum Device Simulations of n -channel MOSFETs and SOI Devices

It has long been held that electron transport in devices is well described by the Boltzmann transport equation which is a continuous, causal, deterministic partial integro-differential equation with no explicit hint of an underlying carrier trajectory description, except in the purely ballistic regime. On the other hand, the Monte Carlo method is intrinsically a kinetic theory that is based upon trajectories in configuration space and a stochastic formalism. In the simulation of ultra-small devices, however, we already encounter the paradox of modeling devices containing, at most, a few hundred electrons with simulations of 10's of thousands of histories of the pseudo-particles in the ensemble. Can a few, say N , Monte Carlo histories really represent the behavior of N carriers in a real device? Indeed, is the BTE appropriate to these devices? The answer to both of these questions is a resounding "no".

In this research proposal, we propose to relax some of the approximations used in deriving the Boltzmann transport equation. We will use the effective potential approach in conjunction with standard Monte Carlo particle-based method when modeling ultra-small MOSFETs and narrow channel SOI devices to take into account space-quantization effect and the quantum-mechanical gate-channel and source-drain tunneling in the narrowest channel devices. More details of this approach are given in Section 4.2.1. Furthermore, we propose to utilize quantum Molecular Dynamics approach based on localized wave-packet description when modeling ultra-small MOSFETs, described in Section 4.2.2. For the case of SOI devices, we will utilize the Landauer scattering matrix approach to properly take into account quantization and Coulomb blockade effects (Section 4.2.3).

4.2.1 The Effective Potential Approach to modeling of n -Channel MOSFETs and SOI Devices

We propose to incorporate various quantum mechanical phenomena within the context of existing EMC particle-based simulation codes for 2D and 3D device simulation already developed as part of an ongoing NSF-CAREER proposal. More precisely, quantum potential framework will be established to account for quantum effects such as quantization of motion, tunneling, and interference effects, basically modifying the classical potential solution coming from the solution of Poisson's equation at each simulation time step, with the addition of a quantum or effective potential. Within the general approach described above, we will specifically address the following critical issues in ultrasmall MOSFETs and SOI devices:

Tunneling - Within the quantum potential approach, tunneling is naturally incorporated as an effective lowering of the tunneling barrier as carriers approach the barrier. This is of particular relevance in short channel n - and p -MOSFETs made in the Si or SiGe technology as the quantum potential lowers the source-channel barrier, which is now recognized as limiting the source-drain current.^{49,50} Alternatively, within the context of particle-based simulation, the transfer Hamiltonian method treats tunneling within a perturbative scheme suitable for implementation within an EMC type approach. In this research proposal we will investigate the applicability of these two approaches for gate-oxide and source to drain tunneling, in terms of their accuracy and required CPU time, on the example of a 25 nm MOSFET device with realistic doping profiles. This will be accomplished in collaboration with the group of Alex Demkov from Motorola, where *ab initio* techniques are currently being utilized to calculate the tunneling rate at the Si-SiO₂ interface.

Scattering - As mentioned above, the proper treatment of scattering within the EMC approach will be investigated, including such effects as the intercollisional field effect (ICFE), and proper incorporation of collision broadening (CB). To address these issues, we will investigate the full scattering kernel of the Wigner-Boltzmann equation for an understanding of the proper treatment of these effects.

Quantization - As already discussed in Section 1.3, quantization effects give rise to consideration of quantum or effective potentials, which may account for some of the important physics occurring, for example, in the inversion channel of MOSFETs, or an SOI device structure. Comparison with full quantum mechanical simulation tools available at ASU will provide important calibration of the effectiveness of quantum potential based approaches to account for this phenomenon. We have done some preliminary investigations in this direction on the example of Silicon wires and have shown that the theoretical value for the standard deviation used in the effective potential approach gives almost identical results for the electron line density when compared to a full 2D Schrödinger-3D

Poisson solver developed at Arizona State University. The results of these simulations, for wire thickness of 7 nm and different wire widths, are shown in Figure 5.

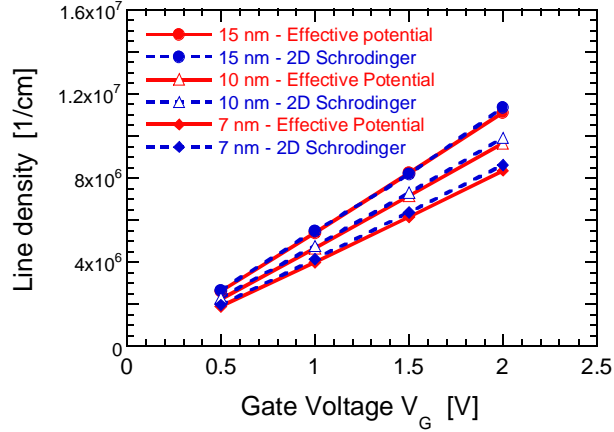


Figure 5. Variation of the line charge density for a quantum wire that represents the channel region of the SOI device structure from Fig. 7. The wire widths equals 7, 10 and 15 nm.

Fluctuations - Potential fluctuations due to discrete impurities and roughness effects have already been shown to be limiting factors in device performance at the ultra-small scales. We are currently investigating such effects through semi-classical schemes. Here, we propose to address quantum mechanical aspects of inhomogeneities in terms of multiple scattering and interference through quantum particle based simulation. Comparison between semi-classical and quantum simulations, and their ability to account for experimental observation of threshold voltage variation, sub-threshold leakage, etc. in research level MOSFETs, will be part of this task. We will also investigate new ways of treating roughness within a Monte Carlo particle-based approach.

To address the above-described issues, we will employ an effective potential scheme in conjunction with a Monte Carlo particle-based simulator. In the Monte Carlo scheme, to estimate the transmission coefficient and the on-state current using the scattering matrix approach due to Lundstrom *et al.*^{51,52,53}, we will simulate a total of N_{sim} particles out of which the number of transmitted particles through the pn -junction is N_t . Then, the incident and the emerging fluxes for the whole junction region will be calculated as $b_2 = N_{sim}v_T$ and $b_0 = N_tv_T$, where v_T is the thermal velocity of the carriers. With the above, we will calculate the reverse transmission rate t' of the composite scattering matrix

$$t' = \frac{b_0}{b_2} = \frac{N_t}{N_{sim}}. \quad (6)$$

Then, using the cascading rule for scattering matrices, we will estimate the backscattering rate for the fluxes incident on the space-charge-region that will allow us to evaluate the current. We will consider thin-width SOI devices with uniform wire width and disordered SOI devices in which we expect to observe Coulomb blockade effects.

4.2.2 Quantum Molecular Dynamics (QMD) Methods Based on Localized Wave Packets for modeling n -channel MOSFETs

Carrier-carrier interactions are thought to play a crucial role in short channel devices, and may even be enhanced in ultra-small geometries.⁵⁴ The existing 3D Monte Carlo particle-based simulator, developed as part of the ongoing NSF-CAREER proposal, which includes a real-space molecular dynamics (MD) routine that prevents the double-counting of the long-range force,⁵⁵ was used to examine the role played by the short-range electron-electron ($e-e$) and electron-ion interactions ($e-i$) on terminal device characteristics for n -channel MOSFETs. To elucidate the importance of these short-range Coulomb interaction terms, on the left panel of Figure 6 we plot the average energy of those electrons that enter the drain end of the device from the channel. Relaxation occurs in the drain over a few nanometers when short-range Coulomb interactions are accounted for via the MD routine. Also, Coulomb "scattering" causes significant shift in threshold voltage as well as a reduction in the actual drain current. The latter is due to the modification of the channel electron mobility via the modification of the distribution function.⁵⁶ These trends are shown in the right panel of Figure 6. On both figures, the mesh force is obtained by solving the 3D Poisson equation.

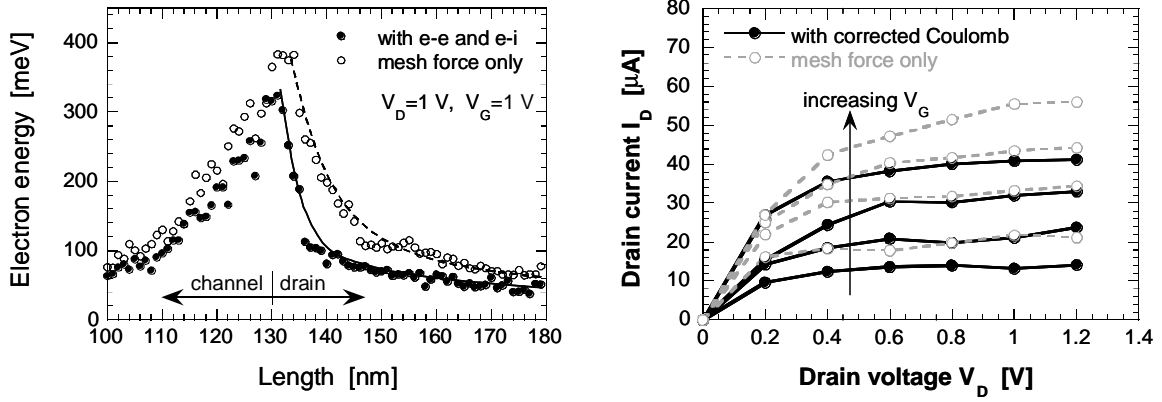


Figure 6. Left panel: average energy of those electrons that enter the drain region from the channel. The simulated test device has channel length $L_G = 80$ nm, channel width $W_G = 80$ nm and oxide thickness $T_{ox} = 3$ nm. The lateral extension of the source and drain regions is 50 nm. The channel doping equals $3 \times 10^{18} \text{ cm}^{-3}$. The applied bias is $V_G = V_D = 1$ V. Right panel: Output characteristics for a device with $L_G = 35$ nm, $W_G = 35$ nm, $T_{ox} = 2$ nm, channel doping $N_A = 5 \times 10^{18} \text{ cm}^{-3}$ in the p -region and $N_D = 10^{19} \text{ cm}^{-3}$ in the source and drain.

The above two examples clearly demonstrate that, for accurate modeling of ultra-small devices, one must properly account for the short-range Coulomb interactions. However, the presently used model is purely classical and treats, in a very simple manner, the core electron contributions. It also requires a large number of particles to be simulated in the source and drain regions. Improvements of the existing model are, thus, mandatory. In addition, when using the smooth effective quantum potentials, for example, to account for space quantization effects, one essentially assumes a fully thermalized system close to equilibrium. In very small structures this assumption might not be applicable, since many-body effects and electron-barrier interaction are much more important than collision dominated processes. We, therefore, propose to develop a new many-body quantum molecular dynamics (MD) approach for device regions that are only weakly or not at all thermalized. We want to point out that the existing quantum MD calculations suffer from the drawback of having to compute higher-order derivatives of density functions, which is usually done using generalized least squares methods. These methods also require a sufficiently high density of computational particles, which severely limits their application in more than one dimension. To overcome these difficulties, we will develop a quantum MD method based on an approximate solution of the many-body Schrödinger equation using localized wave packets with enough degrees of freedom to accurately compute higher density derivatives. The approach taken in quantum chemistry calculations³⁷ uses Gaussians in position-space which move with a velocity given by the phase of the wave function. In principle, there exists a multitude of possibilities to add additional degrees of freedom to this Gaussian description. As the most obvious possibility, we will consider tightly focused Gaussians in position-space, which are modulated by Hermite polynomials. The additional degrees of freedom, given by the coefficients of these Hermite polynomials, can be used to accurately approximate the higher-order derivatives of the wave packet using a Galerkin procedure. This will allow us to use the quantum MD method with much fewer particles, while at the same time retaining all many-body effects in the simulations and without making use of any mean field approximation.

4.2.3 The Transfer Matrix Approach for modeling SOI-Devices

Another approach to modeling the SOI devices discussed in section 4.2.1, is to think of them as quantum wires, a concept from mesoscopic physics well described in textbooks^{57,58}. This viewpoint is particularly useful in the ballistic regime, where most of the scattering comes from the device boundaries. As channel lengths become ever shorter, it becomes increasingly more appropriate to model devices in this manner.

A quantum wire is essentially a waveguide for propagating electron waves. Depending on the electron density and the width of the wire, only a certain number of quantized modes are allowed to propagate. The amount of current that is passed by the device then depends on the transmission probability of these modes. According to the formalism originally developed by Landauer⁵⁹ and extended by Büttiker⁶⁰, the source-drain current, I_{ds} , can be expressed as the integral

$$I_{ds} = \frac{2e}{h} \int (f(E) - f(E - eV_{ds})) \sum_{nm} |t_{nm}(E, V_{ds}, V_G)|^2 dE \quad (7)$$

where V_{ds} is the voltage drop from source to drain, $f(E)$ is the Fermi function for energy E , and t_{nm} is the transmission amplitude going from mode n to mode m and the summation is over all propagating modes. Thus, obtaining the current comes down to computing these quantum mechanical transmission amplitudes. There are a number of different ways for doing this, but a method that we have used with great success^{61,62} is that of Usuki *et al.*⁶³, who

developed an approach based on a numerically stabilized variant of the transfer matrix method. To begin, the Schrödinger equation is mapped onto a finite difference mesh on a square lattice of lattice constant a . Since the wires are of finite width, extending a given number (M) of lattice sites across, one can work in terms of slices, where ψ_j is a M -dimensional vector containing the wave function amplitudes of the j th slice. The discretized Schrödinger equation, keeping terms up to first order in the approximation of the derivative, has the form:

$$(E - \mathbf{H}_j)\psi_j + \mathbf{H}_{j,j-1}\psi_{j-1} + \mathbf{H}_{j,j+1}\psi_{j+1} = 0 \quad , \quad (8)$$

In the above equation, the \mathbf{H}_j matrices represent Hamiltonians for individual slices and the matrices $\mathbf{H}_{j,j-1}$ and $\mathbf{H}_{j,j+1}$ give the inter-slice coupling. By approximating the derivative by finite differences, the kinetic energy terms of Schrödinger's equation get mapped onto a tight-binding model with $t = -\hbar^2/2m^*a^2$ representing nearest neighbor hopping. The potential V at site i,j simply adds to the on-site energies, which appear along the diagonal of the \mathbf{H}_j matrices. Transfer matrices that allow translation from source to drain can be derived using (8). These allow the modes of the wire to be determined (these are the eigenvectors of the transfer matrix of the first slice). Setting the boundary condition that these modes are occupied on the source end with unit amplitude, one obtains the transmission amplitudes that enter (7) by translating across the system. By using some clever matrix manipulations, Usuki *et al.* overcame the problems created by the exponentially growing and decaying contributions of evanescent modes destabilizing the standard transfer matrix approach. Rather than just multiplying transfer matrices together, the translation scheme is turned into an iterative procedure (similar to the cascading scattering matrix approach employed by several other authors^{64,65,66}), which provides numerical stability by not allowing the evanescent contributions to diverge.

Given the transmission amplitudes, the electron wave functions and thus the electron density can be reconstructed quickly via back substitution. This latter point is quite important as there are concerns regarding the feasibility of making such quantum calculations self-consistent. In this regard, it should be mentioned that in an appendix to their paper, Usuki *et al.* demonstrated that their stabilized transfer matrix approach is essentially equivalent to the recursive Green's function method that has already been employed by Datta⁶⁷ to study MOSFETs under non-equilibrium conditions and satisfying self-consistency requirements. As we have found ways to dramatically speed up the reconstruction the wave function over the method originally outlined by Usuki *et al.*, we believe we will be able to perform fully self-consistent quantum mechanical calculations with greater numerical efficiency than Datta's already successful algorithm.

In the case where the SOI device has a significant amount of disorder, the quantum wire analogy breaks down and one expects the device to behave as a chain of electron islands (in other words, quantum dots) connected in series. The method we have described works quite well in the case of coupled quantum dots. However, if the interdot coupling is weak, so that charge transfer occurs only via tunneling, and the number of electrons on each dot is a small, well defined number, then Coulomb blockade effects become an important consideration. Under such conditions, the dots can act like capacitors, such that adding an extra electron to a particular dot requires the cost of a charging energy to be paid in order to overcome the Coulomb repulsion present on that dot. With regards to performing quantum mechanical simulations, the requirement that the charge on each dot be strictly quantized to integer values provides an additional highly nontrivial constraint on the numerical procedure for self-consistency⁶⁸.

4.3 High-Performance Computing

To accelerate the speed of our existing solvers and the ones proposed as part of this research project, we will also work on parallelizing these codes on a Beowulf cluster that was purchased as part of the ongoing NSF and ONR research proposals at Arizona State University, and is currently being installed in the Computational Electronics Lab. For this purpose, we propose to use ideas from Thoule *et al.*⁶⁹ to extend the 3D multigrid solver to handle non-uniform grid spacing. While simple multigrid methods (uniform grid spacing) yield fast initial convergence, they also tend to slow down as the calculation proceeds to a low asymptotic rate. We are planning to investigate the semi-coarsening and directional coarsening methods, as they have been found successful in convection problems, in which Euler's equation is solved.⁷⁰ The multigrid methods can be applied to unstructured meshes by interpolating between a sequence of separately generated meshes with progressively increasing cell size. However, it is not easy to generate very coarse meshes for complex configurations. An alternative approach is to automatically generate coarser meshes by collapsing edges or by agglomerating control volumes. Particle based methods will employ strategies to map sub-ensembles of particles in a load balanced fashion to individual processing elements or nodes. This part of the research will be supported as in the past through collaboration with various supercomputer center facilities such as NCSA.

5. Teaching Activities

Training of graduate students is the central theme of the educational component of this project. The PI will also try to involve as many undergraduate students as possible to work on their Honors Thesis in connection with the project. Also, courses at both the undergraduate and graduate level will be offered in the Electrical Engineering Department at ASU, and these courses will focus on numerical solution techniques used in device modeling. A Web-

based computational toolkit, which will also serve as a depository for codes and class related materials, will be completed as part of an ongoing NSF-CAREER proposal and this research proposal. A more detailed description of each of these tasks is given below.

5.1 Undergraduate Honors Thesis

Under current NSF funded programs of research, the PI has been very proactive in terms of participating in the NSF REU program (Research Experiences for Undergraduates). Three individual REU students were funded over the duration of previous NSF programs. Two of these students continued for their Ph.D. degree at ASU and Kansas State University. Therefore, the PI of this research project has shown a strong record for supporting undergraduate education as part of NSF sponsored research, and attracting students into graduate programs. We will continue this strategy of attracting top students to graduate school through the NSF REU program. One venue that will be followed is via the University's Honors Thesis program. It offers to undergraduate students in the Colleges of Liberal Arts and Sciences and of Engineering and Applied Sciences at Arizona State University the option (with a certain grade point average as a prerequisite) to replace part of their course work by an Honor's thesis. During the spring semester of 2001, we have already identified promising candidates for such an honor's thesis in the appropriate "feeder" courses. While an undergraduate thesis will usually not involve original research, work on an honor's thesis in the context of a group project can take a variety of forms, such as working with other students from the group. The second venue we will pursue will be via the Senior Design Laboratory class, offered on a regular basis in Electrical Engineering Department at ASU, where teams of undergraduates will be recruited for the design of modules such as visualization tools for 3D simulation and graphical interface for I/O.

5.2 Coursework

Courses at both the senior undergraduate and graduate level, in the area of numerical semiconductor device modeling, will also be developed. We have already offered a special topic class in the area of computational electronics in the spring of 1998, which was co-taught jointly by Vasileska and Goodnick. A complete set of the lecture notes was developed for this class (www.eas.asu.edu/~eee598), which is being integrated in the Purdue University Network Computing Hub - PUNCH (<http://www.ecn.purdue.edu/labs/punch>) as part of the DESCARTES-NSF project. This course will continue to be developed and taught by Vasileska, through the distance education program, in particular as part of a recent initiative from the three Arizona Universities to offer a Collaborative Master of Engineering program. Lecture notes for the graduate level Semiconductor Device and Process Simulation class, offered in the Spring of 1999 and Spring 2001, were also developed (<http://www.eas.asu.edu/~eee533/>) and will be integrated into PUNCH. For all the classes taught by the PI (Quantum Mechanics, Semiconductor Transport, Semiconductor Device Modeling, Computational Electronics, Semiconductor Device Physics, Solid State Electronics), visualization tools will be developed in Java to better illustrate to the students the material being taught. An undergraduate level class in numerical semiconductor device simulation will also be developed and offered as part of this research project.

5.3 Preparing Future Faculty

There are a variety of initiatives on the ASU campus that are designed to better prepare our students for employment after graduation. We will coordinate the educational component of this project with these initiatives. Among the more prominent is the Preparing Future Faculty (PFF) program in which students from very different scientific backgrounds share their experiences and are forced to defend the relevance of their research activity to educated laypersons. All the graduate students in the project will participate in the PFF program.

5.4 Web-Based Activities

Besides research and class-related activities, we will continue to work on the development of an on-line computational toolkit, accessible through the Web, which will improve our educational activities, facilitate our research productivity and visibility and lead to new opportunities for outreach. Purdue University has already developed a Computational Electronics Hub and the necessary interface for easy installation and use of the tools from the Web. As part of the existing NSF-CAREER proposal, we will be contributing a number of tools to Purdue's Computational Electronics Hub. At the same time, as part of this proposal, we will continue with the development of a separate Hub at ASU, which will be linked to the one at Purdue. On-line manuals will be provided for the installed simulation tools. Besides simulation tools, we will also make available on our Web-site some of the most representative computer animated sequences which have been made in ASU's Visualization Lab.

5.5 Annual Workshop in Short Courses

As part of this research project, we also propose to establish an annual workshop with short courses targeted to graduate students and engineers in the local industry to educate new generations of computational device researchers on methods for nanoelectronics simulation. The courses will be designed such that the course materials are placed on the Web, so that after the presentation of the course, the materials and the computer tools will be avail-

able to others for self-placed study and to institutions that will be collaborating on this research proposal and have closed their internal universities (Motorola University was closed in the beginning of this year).

5.6 Involvement of Minorities

The PI will also be very active in encouraging bright young women to take Electrical Engineering as their major via the Women in Science and Engineering (WISE) programs at ASU. She has already been actively involved in WISE-TEAMS (middle school) and WISE-UP (high school) programs at ASU and has taught middle school and high school students on such topics as how a motor works, what is digital logic and how one can simulate electrical circuits using SPICE simulators. As part of this research project, the PI will continue to develop new Electrical Engineering Labs, in which, through hands-on activities, the students will learn more about the field of Electrical Engineering.

6. Project Organization and Anticipated Benefits

The expected timeline of accomplishment for the major tasks will be as follows. Completion of the ongoing implementation of the full-band Monte Carlo simulator coupled with a 3D multi-grid solver for modeling SiGe-based p -channel MOSFETs is expected to be completed within the first two years of the grant. The remaining time on this phase will be spent in application and calibration of this tool, enhancement of portability and user interface, parallel implementations (years 1-3), and implementation of quantum corrections (years 2-3) for decreasing geometries. This code is expected to be a mainstay of the program for several years in terms of providing a direct comparison to scaled devices. The influence of the random dopant fluctuations on the device characteristics in scaled Si MOSFETs, used in low-power applications, will be investigated during years 1-2 and will utilize the quantum molecular dynamics methods. Investigation of the operation of the SOI devices using the effective potential approach is expected to yield results in the 2nd year of the program, and full 2D and 3D simulators developed during the 3rd, where benchmarking and comparison to the transfer matrix approach will be performed.

The Computational Electronics class will be offered in the Spring of 2003 and Spring 2004. In the spring of 2003, the PI will also offer an undergraduate class in Numerical Device Simulation to prepare undergraduate students in the challenging field of Computational Electronics. The Annual Workshop in Short Courses will be offered during Summer in years 2003 and 2004. During the whole duration of the grant, the PI will also try to attract top undergraduate students into her research activities. Also, during each summer, the PI will be actively involved in the WISE program, in helping to attract bright female students into the engineering discipline.

The anticipated benefits of this program of research are the development of stable, robust tools, which will allow simulation from current 0.1 μm technology, down to several nanometers for future device technologies. The combination of highly efficient algorithms for solving the 3D Poisson equation, the continued power law improvement in processor speeds and memory, and improved algorithms and communication systems for multiprocessor computing should make the goals of this program of research achievable. The timing for the development of such tools is very appropriate in terms of the critical dimensions being approached now for scaled conventional devices, and during the time period of this research program for future, ultra-small scale alternative device technologies.

7. Industry/University Collaboration

This research proposal will be strongly supported by collaboration with local industries, including Motorola and Intel. It will also allow us to strengthen our collaboration with the Motorola-Austin and Intel-Santa Clara Groups. These industry collaborations are critical in providing calibration data on state of the art devices that can be used to verify our models. The Motorola Group in Phoenix includes Drs. Thoma Rainer, Tom Zirkle, and Alex Demkov, with which we already have strong ties via an ongoing SRC-funded project. Issues that are of interest to both ASU's and Motorola Group include: gate leakage in thin oxides, source to drain tunneling, and the inclusion of quantum potentials in classical device simulators, used on an every day basis in Motorola. Prof. Vasileska has helped Alex Demkov in organizing the *Workshop on Computational Materials and Electronics*, which was held in Tempe, Arizona, in November 1999, 2000 and 2001. Vasileska is also on the Program Committee of the *International Conference on Modeling and Simulation of Microsystem* (co-sponsored by Motorola), and has organized several special sessions on quantum transport modeling of future ultra-small devices. The Intel Group from Santa Clara includes Drs. Tom Linton (Industrial Liaison for the ongoing SRC project). This group is particularly interested in non-equilibrium transport models for the end-of-the-roadmap devices that include quantum effects. The Intel would like to participate and help with this proposal by allowing students to spend the summer at Intel for alpha-testing of our codes using Intel device data. To make the Courses offered by ASU available to the large number of students working part-time or full-time in the local semiconductor industry, the PI will continue to be actively involved in the development of Web-based and distance learning classes. This will be accomplished via ASU's College of Extended Education with its resources which allow these off-site students to participate in class from their work place.