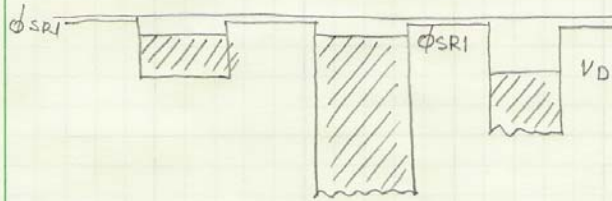
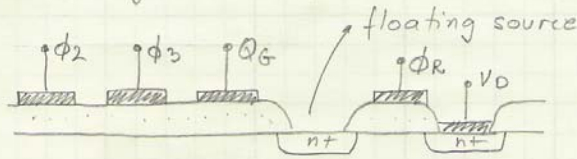


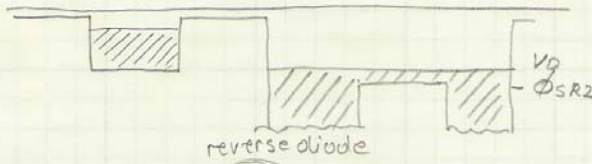
charge output

- The charge output is slightly more complicated than the charge input. For this purpose, one has to imagine the CCD as a delay line. The input voltage has been converted into charge packets. Suppose that at some instance of time, one of them is located under gate 3 as a signal charge.

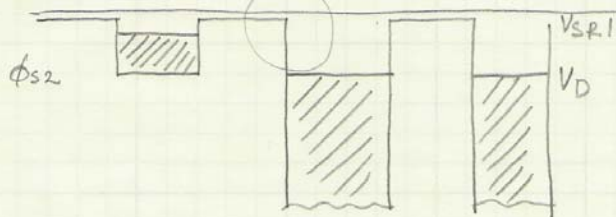


- output circuit consists of an output gate and a MOSFET with a floating nt source, a reset gate ϕ_R and a drain bias to the dc-voltage V_D .

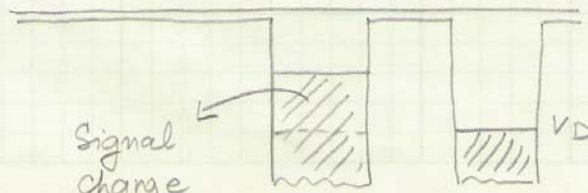
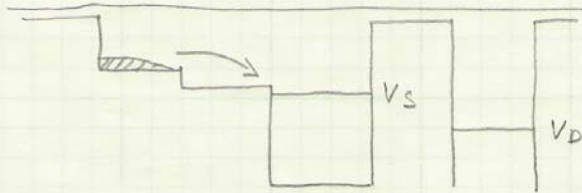
- A short reset pulse applied to ϕ_R , changes its surface potential from ϕ_{SR1} to ϕ_{SR2} . When $\phi_{SR2} > V_D$, the surface potential change above V_D will flow into the drain.

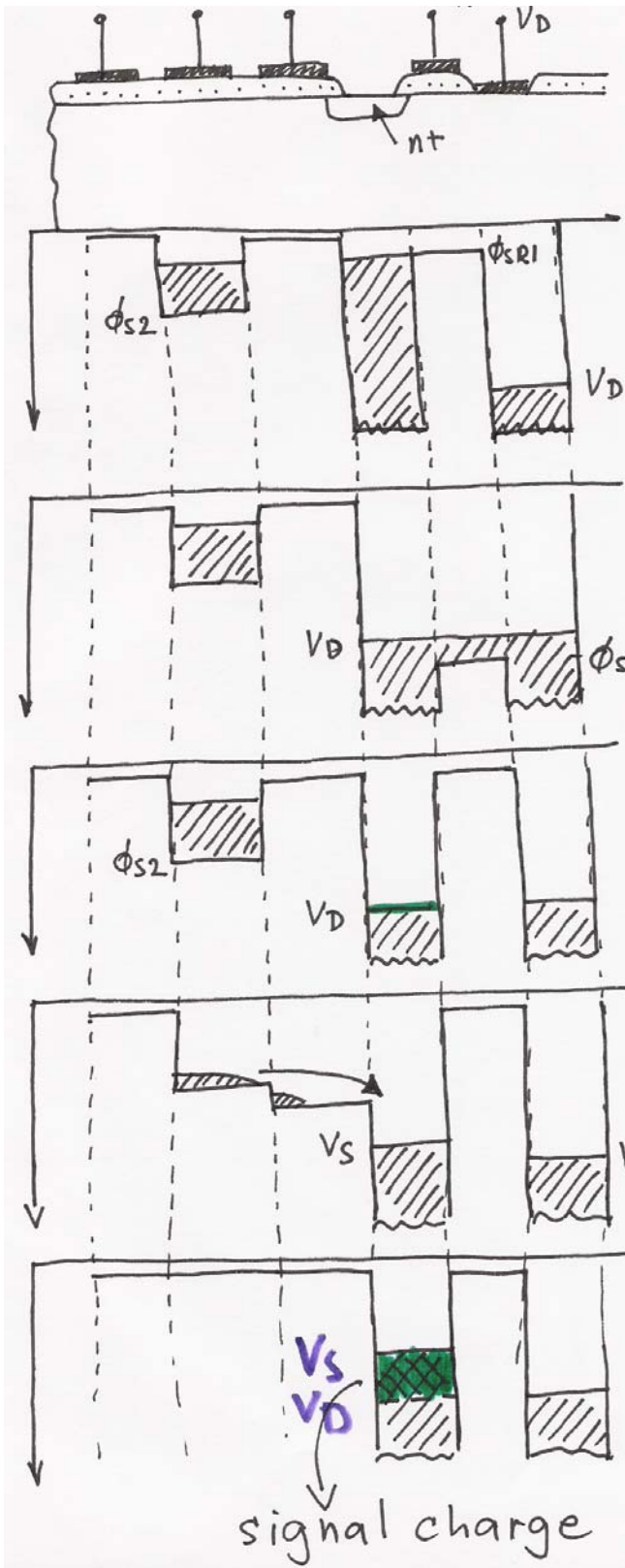


- At the end of the reset pulse, the surface potential under the reset gate returns to its equilibrium value but the island (float) remains at V_D . Through this reset operation there is now reverse biased diode that is isolated.



- Pulsing the output gate above ϕ_{S2} allows the charge to flow into the floating diode, lowering its potential to V_S .





$t = t_0$
 charge packet under
 gate 3
 "signal charge"

↓ short reset pulse

$$\phi_{SR2} > V_D$$

↑
 ϕ_R returns to original
 value

↓ pulse output gate

↓ output gate
 pulsed back

$$\Delta V = \frac{QN}{C} = V_D - V_s$$

ΔV - potential
 drop in floating
 diffusion

