



Charge transfer

- The assumption so far is that charge transfer from one potential well to the next to be perfect. In reality charge transfer is imperfect due to:

- (1) Insufficient time for charge to flow from well to well
- (2) some charge is captured by interface states
- (3) There may be potential barriers between the wells.

- The effectiveness of charge transfer is expressed by either charge transfer efficiency η or charge transfer inefficiency ϵ , where:

$$\eta = 1 - \epsilon$$

When there is charge loss λ , then:

$$\eta = 1 - \epsilon - \lambda$$

Charge loss occurs when during device operation the surface becomes accumulated and carriers are allowed to recombine with minority carriers captured by interface states.

- The charge transfer process is characterized by the charge transfer inefficiency per elemental transfer, which is the fraction of charge left behind when charge is transferred from one well to the next. Sometimes charge transfer inefficiency per stage is used. Use the following definitions:

- ϵ = charge transfer inefficiency per elemental transfer
- n = number of elemental transfers
- N = number of stage transfers
- d = charge transfer inefficiency per stage.

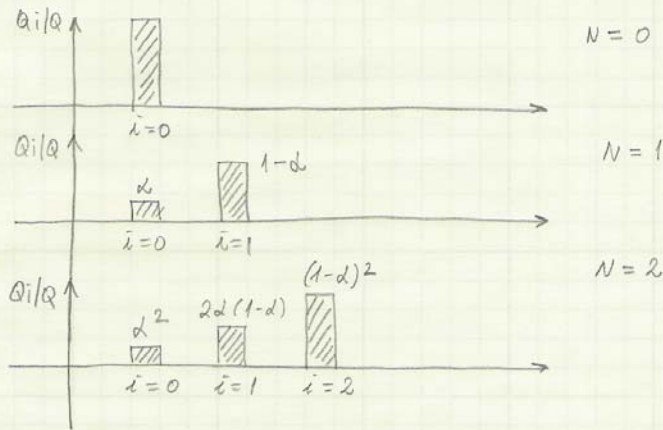
P = number of clocking phases.

Then: $d = PE$ and $n = P \cdot N$.

- Consider a charge in a potential well. After N transfers, the charge is no longer localized in one well, but due to charge transfer inefficiency, it spreads out over several trailing wells. The charge distribution in these wells is then:

$$D_{i,N} = \frac{Q_i}{Q} = \frac{N! (1-d)^i d^{N-i}}{(N-i)! i!}$$

where i is the stage number, $i=0$ being the stage containing the main part of the charge, $i=1$ being the next stage and so on.



The above figure shows the charge trailing due to the charge transfer inefficiency. Note the decreasing size of charge packet with transfer. The charge deficit from the leading charge is found in the trailing packets.

- The fractional deficit from the original charge packet after N -stages transfers is given by:

$$\text{Deficit} = 1 - D_{N,N} = 1 - (1-d)^N = 1 - (1-PE)^{n/P} \approx Nd =$$

The word deficit here means the charge loss from the leading charge packet that is found in the trailing packets.

- The transfer inefficiency has two effects:
 - (1) charge loss from the leading packet
 - (2) charge mixing when there is a followup charge

Example

- Consider a 500 stage three-phase digital delay line in which threshold levels are such that 50% of full charge or more corresponds to a 1 and less than 50% to a 0. For $\epsilon = 10^{-4}$, the charge after 1500 transfers is:

$$(1 - 3 \times 10^{-4})^{500} = 0.86$$

Now if the input charge is not a full well but 80% of a full well. The output is then:

$$0.86 \times 0.8 \approx 0.7$$

If the inefficiency increases to 3×10^{-4} then

$$1 - \text{loss} = 0.64$$

and the output is $0.64 \times 0.8 \approx 0.51$. Thus, the transfer inefficiency has blurred the ability to discriminate between logic values for digital information.

- For analog signals the situation is worse because there are no threshold values. Transfer inefficiency leads to crosstalk. After N stage transfers, the crosstalk between adjacent stages appears as a smeared image in the display. Then:

$$D_{N-1,N} / D_{N,N} = \frac{Nd}{1-d} = \frac{n\epsilon}{1-p\epsilon}$$

Considerable crosstalk reduction is effected if charge is held in every second stage, keeping an empty well between charge packets. Then:

$$D_{N-2,N} / D_{N,N} = [N(N-1)/2] / [d/(1-d)]^2$$

For the transfer inefficiencies of the digital delay line, we find 15% and 45% crosstalk for charges in adjacent stages and 1.1% and 10% when an empty well is provided between charge packets.