

SEMICONDUCTOR MEMORIES



Digital Integrated Circuits

Memory

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Chapter Overview

- **Memory Classification**
- **Memory Architectures**
- **The Memory Core**
- **Periphery**
- **Reliability**

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Semiconductor Memory Classification

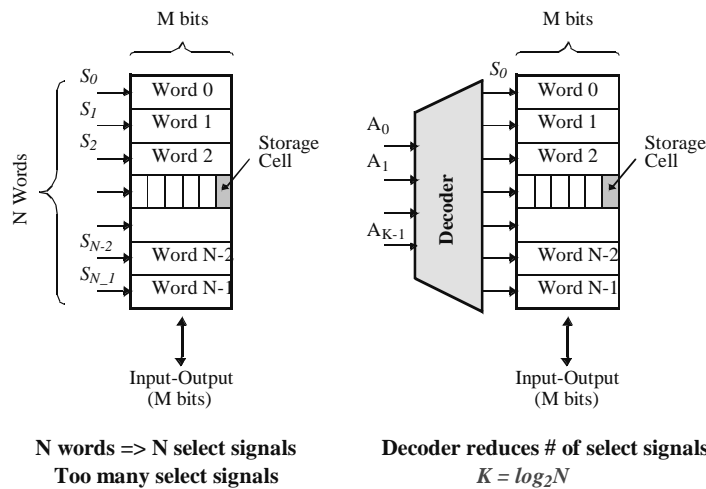
RWM		NVRWM	ROM
Random Access	Non-Random Access	EPROM E ² PROM FLASH	Mask-Programmed Programmable (PROM)
SRAM DRAM	FIFO LIFO Shift Register CAM		

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Memory Architecture: Decoders



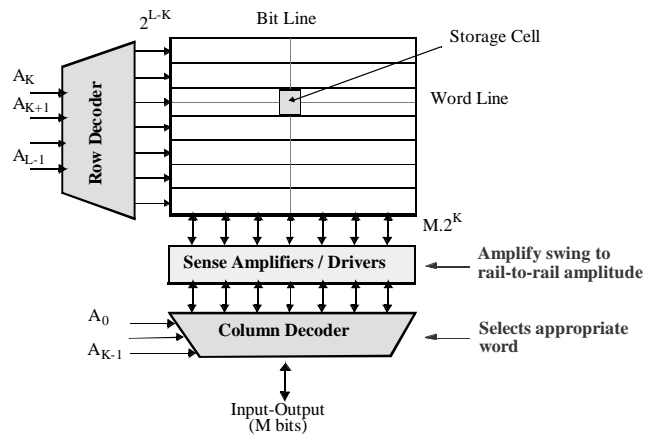
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Array-Structured Memory Architecture

Problem: ASPECT RATIO or HEIGHT \gg WIDTH

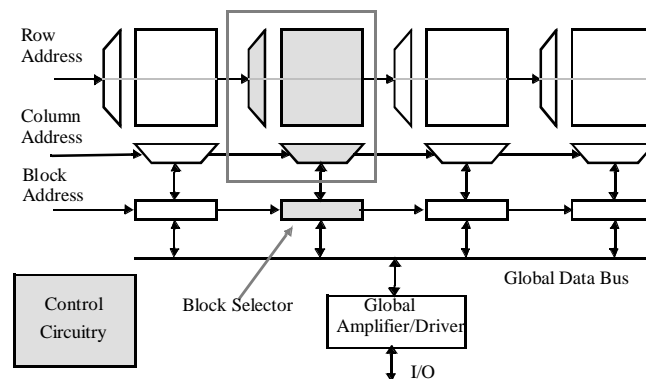


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Hierarchical Memory Architecture



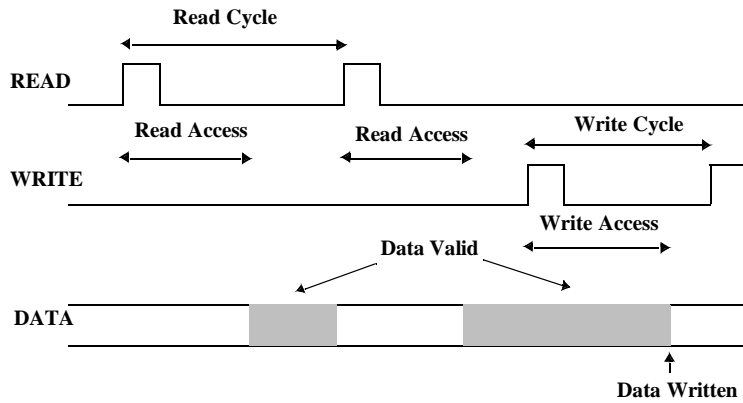
- Advantages:
1. Shorter wires within blocks
 2. Block address activates only 1 block \Rightarrow power savings

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Memory Timing: Definitions

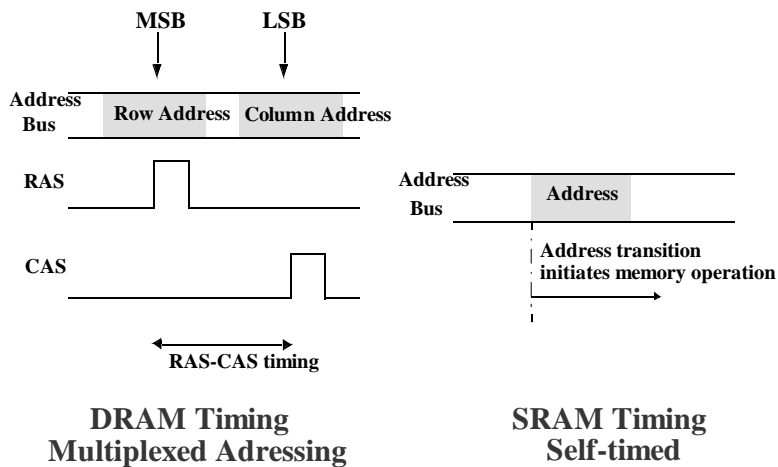


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Memory Timing: Approaches

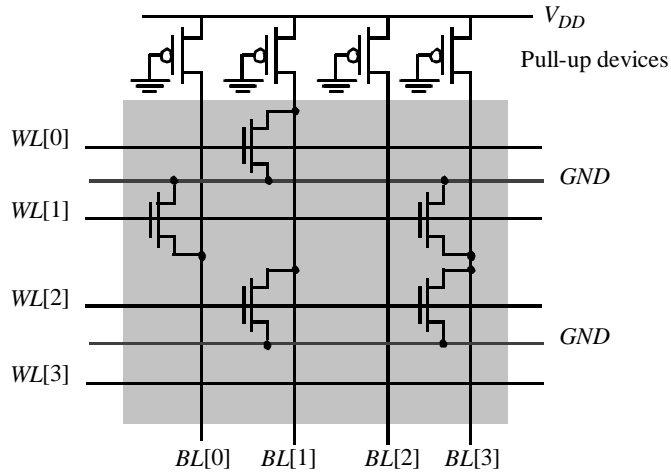


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MOS NOR ROM

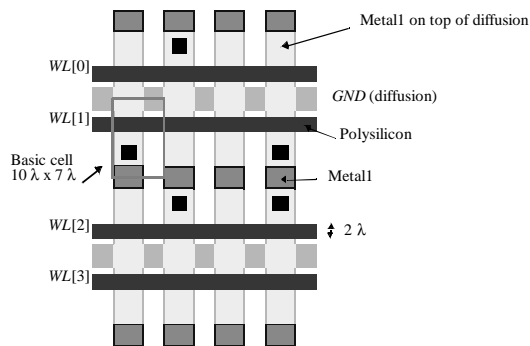


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MOS NOR ROM Layout



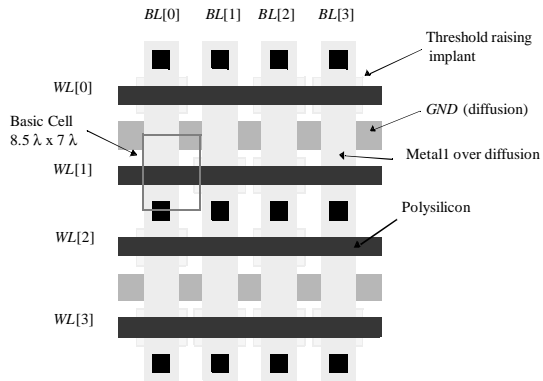
Only 1 layer (contact mask) is used to program memory array
Programming of the memory can be delayed to one of
last process steps

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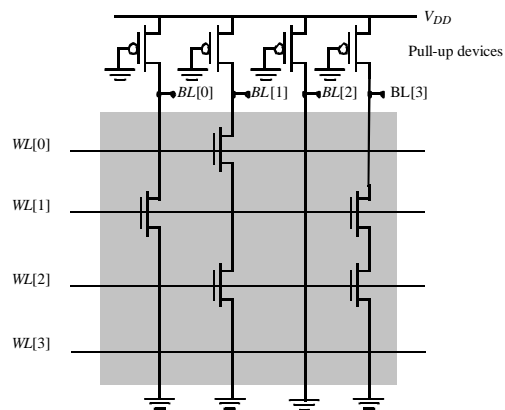
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MOS NOR ROM Layout



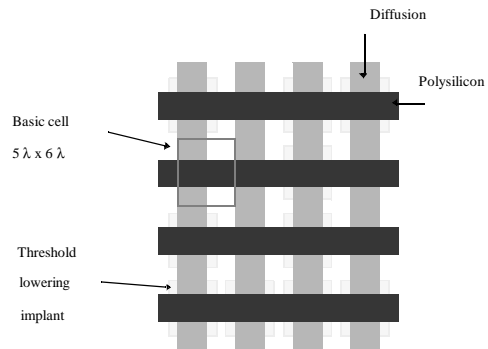
Threshold raising implants disable transistors

MOS NAND ROM



All word lines high by default with exception of selected row

MOS NAND ROM Layout



**No contact to VDD or GND necessary;
drastically reduced cell size**
Loss in performance compared to NOR ROM